NOTE

This manual documents the Model 6070A/6071A and its assemblies at the revision levels shown in Appendix A. If your instrument contains assemblies with different revision letters, it will be necessary for you to either update or backdate this manual. Refer to the supplemental change/errata sheet for newer assemblies or to the backdating sheet in Appendix A for older assemblies.

6070A
6071A

Synthesized RF Signal Generators

Service Manual

P/N 578054
JANUARY 1982

FLUKE®

WARRANTY

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In the event of failure of a product covered by this warranty, John Fluke Mfg. Co., Inc., will repair and calibrate an instrument returned to an authorized Service Facility within 1 year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. With regard to any instrument returned within 1 year of the original purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident, or abnormal conditions of operations, repairs will be billed at a nominal cost. In such case, an estimate will be submitted before work is started, if requested.

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If any failure occurs, the following steps should be taken:

1. Notify the JOHN FLUKE MFG. CO., INC., or nearest Service facility, giving full details of the difficulty, and include the model number, type number, and serial number. On receipt of this information, service data, or shipping instructions will be forwarded to you.

2. On receipt of the shipping instructions, forward the instrument, transportation prepaid. Repairs will be made at the Service Facility and the instrument returned, transportation prepaid.

SHIPPING TO MANUFACTURER FOR REPAIR OR ADJUSTMENT

All shipments of JOHN FLUKE MFG. CO., INC., instruments should be made via United Parcel Service or "Best Way"* prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

CLAIM FOR DAMAGE IN SHIPMENT TO ORIGINAL PURCHASER

The instrument should be thoroughly inspected immediately upon original delivery to purchaser. All material in the container should be checked against the enclosed packing list. The manufacturer will not be responsible for shortages against the packing sheet unless notified immediately. If the instrument is damaged in any way, a claim should be filed with the carrier immediately. (To obtain a quotation to repair shipment damage, contact the nearest Fluke Technical Center.) Final claim and negotiations with the carrier must be completed by the customer.

The JOHN FLUKE MFG. CO., INC, will be happy to answer all applications or use questions, which will enhance your use of this instrument. Please address your requests or correspondence to: JOHN FLUKE MFG. CO., INC., P.O. BOX C9090, EVERETT, WASHINGTON 98206, ATTN: Sales Dept. For European Customers: Fluke (Holland) B.V., P.O. Box 5053, 5004 EB, Tilburg, The Netherlands.

*For European customers, Air Freight prepaid.

John Fluke Mfg. Co., Inc., P.O. Box C9090, Everett, Washington 98206

Rev. 8/81

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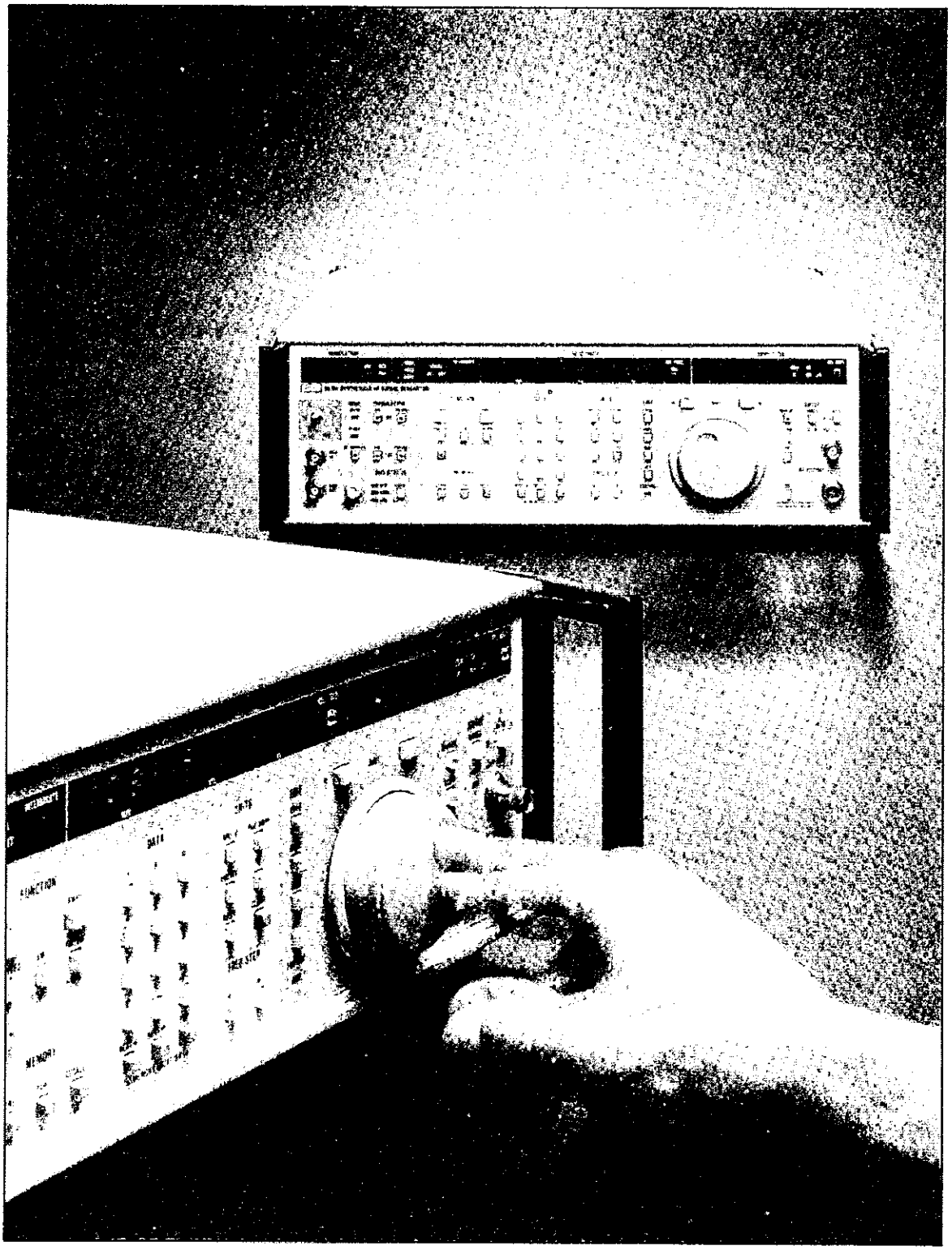

6070A/6071 Synthesized RF Signal Generators

Section 1
Introduction

1-1. THE MANUAL SET

1-2. The John Fluke Models 6070A and 6071A RF Synthesized Signal Generators are documented by a set of four manuals: the 6070A/6071A Operator Manual, the 6070A/6071A Calibration Manual, the 6070A/6071A Service Manual, and the 6070A/6071A Schematics Manual, (Figure 1-1). The 6070A/6071A Operator Manual introduces the instrument; familiarizes the operator with all instrument controls, connections, and indicators: and presents detailed operating information. The 6070A/6071A Calibration Manual provides procedures for general maintenance, performance checks, and calibration adjustments. The 6070A/6071A Service Manual describes the theory of operation and troubleshooting and includes a list of replaceable parts. The 6070A/6071A Schematic Manual contains a functional block diagram, a wiring diagram, and all schematic diagrams of the instrument.

1-3. The major difference between the 6070A and the 6071A is that the 6071A has twice the upper frequency limit of the 6070A. Because of the similarity of the models, most of the text in this manual applies to both the 6070A and the 6071A. Text that applies to just the 6070A or just the 6071A is identified as such.

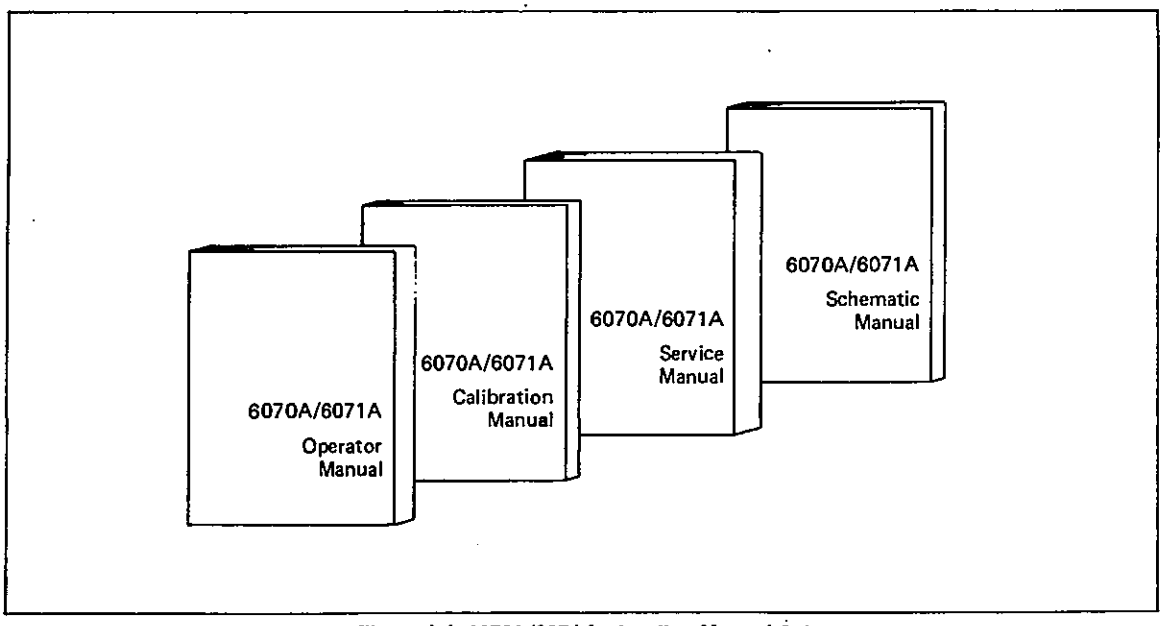

Figure 1-1. 6070A/6071 Instruction Manual Set

1-4. THE 6070A/6071A SERVICE MANUAL

1-5. The information in this, the 6070A/6071A Service Manual, is divided into eight sections:

1 INTRODUCTION
Introduces the 6070A/6071A Instruction Manual set and the 6070A/6071A Service Manual.

2 THEORY OF OPERATION
Describes the theory of operation under three headings: Software, Theory of Operation, and Circuit Analysis.

3 ACCESS PROCEDURE
Describes the procedures necessary to gain access to each major assembly and to gain access to each circuit board inside the instrument.

4 TROUBLESHOOTING
Contains troubleshooting information that aids the technician in locating an indicated trouble to a particular assembly.

5 NONROUTINE ADJUSTMENT PROCEDURE
Describes Non-routine Adjustment Procedures. These maintenance procedures are usually performed after removal and replacement of circuit board components.

6 LIST OF REPLACEABLE PARTS
Contains the list of replaceable parts for the 6070A and the 6071A.

7 OPTIONS
Contains the Options Access Procedures.

8 BACKDATING
Contains addenda and manual change information.

1-6. LIST OF RECOMMENDED TEST EQUIPMENT

1-7. The test equipment recommended for servicing the 6070A/6071A is listed in Section 1 of the 6070A/6071A Calibration Manual. If the recommended test equipment is not available, equivalent test equipment can be used.

1-8. 6070A/6071A SPECIFICATIONS

1-9. The 6070A/6071A specifications are contained in Section 1 of the Calibration Manual.

1-10. FLUKE SALES AND SERVICE CENTERS

1-11. A list of Fluke Sales and Service Centers is located in Appendix A of the 6070A/6071A Calibration Manual.

1-12. SHIPPING AND SERVICE INFORMATION

1-13. Shipping and service information is contained in Section 2 of the 6070A/6071A Calibration Manual.

Section 2
Theory of Operation

2-1. INTRODUCTION

2-2. This section describes the theory of operation of the Models 6070A and 6071A RF Synthesized Signal Generators. The text is divided into three major headings: Software Operation, Hardware Operation, and Detailed Circuit Descriptions. The Software Operation material provides a general description of the software and a description of how the software controls the hardware. The Hardware Operation material provides a general description of the hardware. The Detailed Circuit Description material provides more detailed description of the more complex circuits.

2-3. SOFTWARE OPERATION

2-4. Introduction

2-5. The 6070A and the 6071A are completely programmable via the IEEE-488 compatible interface. The IEEE-488 messages not only duplicate the function of all front panel controls (Except POWER, CLEAR DATA, and MOD OUT) but also command instrument functions not available from the front panel controls.

2-6. Data can be rapidly transferred between the IEEE-488 compatible interface and the signal generator memory. Characters can be processed as received or as a string, at the programmer's discretion. Serial poll service requests can be selectively masked as needed.

2-7. The interface features front panel monitoring of remote, address, and SRQ status. The bus address can be displayed for use in setting rear panel address switches or checking the current bus address.

2-8. The programming format corresponds closely to that used for manual front panel control, making remote operation easy for systems applications. The 6070A/6071A Operator Manual delineates the programming format.

2-9. Both the 6070A and 6071A rely on a 16-bit microprocessor (Texas Instruments, Inc., TMS 9900) to provide special instrument functions and to perform a variety of self-tests. When the instrument is turned on, the microprocessor controller enables the 6070A/6071A to automatically perform a functional self-check, then go to programmed safe power-up setups. The optional nonvolatile memory enables the instrument to turn on at the previous power-down settings. Other special functions, under control of the controller, allow the user to test the instrument's displays and annunciators, to run a pattern-random-access memory check, to check the nonvolatile memory, and to set or reset the status request line.

2-10. The internal controller also alerts the operator when an invalid entry or a parameter outside the instrument's specified range has been programmed. If an incorrect entry is attempted, the entry is rejected and annunciated. The error can be displayed and identified by pushing an interrogate button. If the user programs a parameter outside of the instruments specified range, this is also annunciated. Pushing the interrogate button causes the appropriate error code to be displayed. See the pullout card located beneath the front panel or Section 5E of the 6070A/6071A Operator Manual for error code interpretation.

2-11. The 6070A and 6071A each contain a built-in memory that allows up to nine (50 with the nonvolatile memory option) front-panel setups and test sequences to be stored and recalled. Test sequences may be stepped through one memory location at a time. An editing feature allows the insertion or deletion of program steps during development. In all, each instrument contains 32K bytes of program read-only memory (RAM), 2K bytes of random-access memory (ROM), a 16K bytes of erasable PROM, the IEEE-488 interface logic, an input/output port and interrupt-handler chip, and the power-on and clock circuitry.

2-12. Software Function

2-13. The system software performs three main functions:

1. It implements a collection of user-programmable functions that are directed towards signal-generator applications.

2. It selects and configures the appropriate hardware building blocks to produce the required output and then linearizes and compensates the signal path to optimize quality and resolution.

3. It implements an extensive set of self-test and diagnostic functions.

2-14. The software package operates as a simple timesharing system where the different instrument functions use the resources of a common CPU in an independent fashion but share communication links and utility routines.

2-15. Software at Work

2-16. At power-on, the software performs instrument self-checking and initializes both the RAM and the instrument hardware at power-on. Then the operating system is booted by loading a RAM-based task table from ROM. The task table contains six frames, each consisting of four words and each word corresponding to a task. The first word points to the microprocessor register workspace in RAM, the second points to the task-program counter, the third contains the processor status word, and the fourth points to the task stack. Once the task table is initialized, multitasking is initiated and the operating system is invoked. The instrument is now fully operational.

2-17. At the heart of the operating system is the task scheduler. The scheduler is actually a subroutine that returns to a routine different from the one that called it. The operating system is not a typical time-slice system, where an interrupt causes transfer of control from one task to another at a predetermined rate.

2-18. In the generator the tasks execute sequentially. The transfer of control between each task happen at well defined points. The operating system supports four primitive functions: suspend, resume, and two binary operations on semaphores, P and V, that implement mutual exclusion.

2-19. The suspend function is a call to the scheduler to save the current task frame in the task table. Because the scheduler operates in a round-robin fashion the suspension of a task always triggers the resumption of the next task in the queue. When invoking the suspend operation, a task may specify a period of time during which it cannot be activated. For example, if the sweep task wants to lift the recorder pen to retrace, it merely commands the pen to lift and then suspends for a period of 200 ms.

2-20. The resume operation performed by the scheduler involves the restoration of the workspace pointer, program counter, status register, and stack pointer for the next task.

2-21. The final two operations are used to resolve contention problems when a task's objective is to update a critical item without interfering with the data until the task is through updating the item. To do so, critical data items are recognized and assigned semaphores in the software design phase. When the generator is running, the state of these semaphores is controlled by the two operations: P, the block operation, and V, the unblock operation. These operations are shown in Table 2-1.

2-22. Each of these operations are time-indivisible. The P operation is sufficient to block access by other tasks, while the V operation unblocks the data. It should be noted that these operations are implemented with very few statements.

2-23. Software Management of the Hardware

2-24. INTRODUCTION

2-25. The following paragraphs give an overall view of how the hardware is managed by the software. The operating software controlled by the IEEE-488 interface is discussed in the Operator Manual.

2-26. SPECIAL FUNCTION ENTRIES

2-27. Special function entries allow the operator to control some special features of the 6070A and 6071A. There are ten classes of special functions. The special functions are described in detail in Section 5E of the 6070A/6071A Operator Manual.

Table 2-1. Semaphore Operations

```
P$   abs   s     ;tests and makes positive (block access)
     jlt   G$    ;if data was unblocked, jump to continue
     suspend     ;else access is blocked, suspend
     jmp   P$    ;loop back and check again
G$               ;continue
```

```
V$   seto  s     ;make s negative (unblock)
```

2-28. To make a special functional entry the operator presses SHIFT and then presses two digits. The first digit specifies the special function class and the second digit specifies the mode of the particular special function. The digits appear in the center of the frequency display. The second digit of the special function entry terminates the entry and returns the instrument to the entry mode corresponding to the last function prefix specified.

2-29. FREQUENCY RANGES

2-30. The frequency range of the 6070A is broken into seven bands. The 6071A has an additional four bands to double the frequency range. Table 2-2 lists the frequency band ranges.

2-31. For all keyboard entries, the instrument autoranges to select the appropriate band. When editing frequency with the knob, the instrument also autoranges unless the fixed range mode is enabled. If fixed range is enabled, the operator may edit frequency only within the confines of the current frequency band, plus an overrange above and below the band endpoints (see Table 2-2). This allows the instrument to be operated around a band switch point without changing ranges (and thus producing an output transient). Note that fixed range applies only to the edit knob, so that reprogramming frequency via the keyboard while fixed range is in effect will still redefine the current band.

2-32. FREQUENCY PROGRAMMING

2-33. Frequency programming is a multi-step process. Because the modulation and amplitude hardware is frequency dependent and must be reprogrammed whenever frequency changes, frequency programming can alter nearly every hardware setting within the instrument.

2-34. The first step in frequency programming is to add the offset frequency to the non-displayed base frequency to produce the new desired output frequency. If this output frequency is within the absolute hardware capabilities of the instrument, it is then coverted into a frequency band number and an equivalent fundamental frequency. All output frequencies originate as a fundamental frequency in the range of 250 ro 520 MHz. This fundamental frequency is then divided by 1, 2, 4, or heterodyned to produce the desired output. In the 6071A the fundamental frequency is doubled to produce the 520 MHz to 1040 MHz band.

2-35. If fixed range is in effect and the knob is used to edit frequency, then the frequency band is fixed at its current value. If the new frequency cannot be accomodated within the current band (or its overrange window), it will not be programmed (see Table 2-2).

2-36. The frequency uncal status condition is set whenever the frequency synthesis hardware is forced into an overrange region. This can occur idependently or in combination with the times two band filters, the frequency band (Mod/Divider filters), or the fundamental frequency synthesizer. Each has an associated binary weighting factor in the uncal code.

2-37. The next step in frequency programming is the updating of uncal status regarding AM modulation rate limitations. Since the maximum AM modulation rate is a function of frequency, it is possible to exceed this limitation when a frequency change occurs.

2-38. Angle modulation hardware is updated next. Because this hardware is closely tied to the frequency synthesis circuitry, a change in frequency programming (especially a change in Mod/Divider band or a crossing of the het band boundary) may require a complete reprogramming of modulation control bits. This step is omitted if angle modulation is disabled, as this step would have no effect on the output of the instrument.

Table 2-2. Frequency Band Ranges

	UNDER RANGE	CALIBRATED MINIMUM	CALIBRATED MAXIMUM	OVER RANGE
(6070A and 6071A)	(0.1)	0.2	62.499999	(64.999999)
	(60.0)	62.5	89.999999	(91.999999)
	(87.0)	90.0	124.999999	(126.999999)
	(120.0)	125.0	179.999999	(184.999999)
	(175.0)	180.0	249.999999	(254.999999)
	(254.0)	250.0	359.999999	(364.999999)
	(355.0)	360.0	519.999999	(525.999999)
(6071A ONLY)	(500.0)	520.0	599.999998	(619.999998)
	(580.0)	600.0	719.999998	(729.999998)
	(710.0)	720.0	874.999998	(894.999998)
	(855.0)	875.0	1039.999998	(1051.999998)

2-39. At this point the actual programming of frequency hardware takes place in terms of the equivalent fundamental frequency. The output sequence is chosen to minimize transients when changing from one frequency to another. The A4A7 Output Amplifier or the A4A6 Times Two Output Amplifier is programmed early in the sequence since it may involve the switching of a relay. This is followed by programming of the A4A4 Modulator Divider band code. Next the KV, CULC, and KN DACs are updated, the PI bits are programmed, and the PH and NI DACs are given new values. The A3A4 N/1 Divider and theA3A7 Sub-Synthesizer are programmed to the fundamental frequency minus a 201-kHz offset. The low-order 4 digits are programmed in BCD, followed by 1 digit in 9's complement, BCD followed by 1 1/4 BCD digits. The remaining digits are programmed in a BCD code.

2-40. The final step is calculation of an amplitude correction factor for the new frequency. This factor compensates for level inaccuracies which are frequency dependent. Paragraph 2-41 discusses the amplitude correction process in detail.

2-41. AMPLITUDE PROGRAMMING

2-42. Amplitude is programmed using a 23 step-(6 dB per step) attentuator, a switched 6 dB amplifier, and a 12-bit vernier DAC. In general the value of the output amplitude can be represented by the following expression:

$$\text{Amplitude (volts)} = 2^n D/1840$$

2-43. Where D = (uncorrected DAC) * (interpolated, normalized correction factor) and n = the total amount of attentuation as an integer multiple of 6 dB (ranges from 1 to -23).

2-44. If the amplitude is greater than 13 dBm when the frequency is below 520 MHz (or 6.9 dBm if the frequency is above 520 MHz), then n is positive and the 6 dB amplifier is turned on. Otherwise n is zero for amplitudes between 7.1 dBm and 13 dBm below 520 MHz (or 1.0 and 6.9 dBm above 520) or negative at or below 6.9 dBm below 520 MHz (or below 0.9 dBm above 520 MHz). If AM is on, the amplitude range corresponding to each n is 6 dB lower than stated above.

2-45. The amplitude correction is a factor which compensates for level inaccuracies and is a function of frequency and attenuator setting. For example, the output circuitry exhibits increasing attenuation as a function of frequency. The amplitude correction compensates for this by increasing the amplifier gain accordingly. Likewise, the amplitude correction can compensate for absolute errors in the attentuator pads because each pad combination is characterized separately in the matrix of correction factors.

2-46. Correction factors are 8-bit unsigned positive integers. They are stored in the calibration EPROM is a 25 by 25 matrix so that they may be changed when the instrument is serviced or calibrated. These correction factors are calculated values based on individual measurements of each attenuator section. In addition to the 25 by 25 matrix of correction integers, there is a single offset variable also stored in the EPROM.

2-47. The first step in programming amplitude is to calculate the attenuator (or amplifier) setting. This calculation is based on the value of the output amplitude. The calculation remains unchanged regardless of the magnitude of the amplitude loss correction and only depends on whether or not the output frequency is below 520 MHz. This feature not only lengthens the life of the attentuator relays, but also makes the output much more usable and freer of transients because the attenuator relays are not exercised when frequency is changed unless the 520-MHz boundary is crossed.

2-48. For the calculated attenuator setting, the corresponding EPROM correction factor is added to the offset, and a piecewise linear interpolation is then performed between two frequency points to obtain the interpolated correction value. The interpolation is carried out with 10-bit resolution to minimize the step size as the correction value increases. The interpolated correction is then normalized and used to compute the corrected DAC value.

2-49. The amplitude DAC has 12 bits of resolution. It can be thought of as being divided into different level segments. The top 7 dB covers the DAC values between 4095 (max DAC value) and 1840, the next 6 dB covers the values 1839 to 920, the next 6 dB covers the values 919 to 460, and so on.

2-50. The top 7 dB segment is reserved for amplitude correction. The normal amplitude vernier uses the next 6-dB segment when AM is off and the second 6-dB section when AM is on. The output amplitude of the instrument is considered to be calibrated (quality is guaranteed) whenever the uncorrected DAC falls within the range of 1840 to 460.

2-51. The absolute minimum value the DAC can assume is 100 (38 mV) and is based on the minimum level the level detector can track. If the amplitude selected requires the DAC to assume values greater than 4095 or less than 100, the DAC is programmed to 4095 or 100 and the AMPL UNCAL annunciator is flashed.

2-52. The sequence in which the attentuators (or amplifier) and DAC are programmed is important. To prevent amplitude overshoots that could damage external circuitry, the 6070A and 6071A first program the combination of the current and previous attentuation

followed by the current DAC setting, followed by the current attentuator setting. This sequence of amplitude programming can cause up to 6-dB undershoot (except when the relay contacts are in transient), but no overshoot.

2-53. AMPLITUDE MODULATION PROGRAMMING

2-54. The 6070A and 6071A allow amplitude modulation depth programming from 0 to 99.9 percent with 0.1 percent resolution. Amplitude modulation depth can be programmed either through a front panel button entry, remote IEEE bus, or front panel knob. When the combination of signal amplitude and AM depth exceeds 19 dBm peak (13 dBm for fout $>$ 520 MHz) the AMPL UNCAL annunciator lights to warn the operator that the output amplitude is no longer guarenteed. Below 520 MHz the maximum calibrated AM depth is 89.9 percent. Above 520 MHz the maximum calibrated AM depth is 69.9 percent.

2-55. The AM modulation frequency 3-dB bandwidth points are defined as 8 kHz for output frequency $\leq$5 MHz and as 50 KHz for output frequency $\geq$5 MHz. When either condition is violated with AM enabled, the modulation frequency MOD UNCAL annunciator lights.

2-56. Amplitude modulation depth is programmed using a 10 bit DAC, with 1000 on the DAC corresponding to 100 percent AM.

2-57. ANGLE MODULATION PROGRAMMING

2-58. Angle modulation is displayed in the 6070A/6071A front panel MODULATION display field with three digits of resolution. This display field is also shared by modulation frequency and amplitude modulation. To select and display angle modulation, the operator must press the angle modulation function prefix button FM/ϕM.

2-59. The instrument allows both frequency modulation (FM) and phase modulation (ϕM). Frequency modulation is displayed with kHz "DEV" units and phase modulation is displayed with "Rad" units. Conversation between FM and ϕM is allowed and is based upon the frequency of the internal modulation oscillator. The conversion relationship is:

$$\text{Frequency Modulation} = (\phi\text{M}) * (\text{Modulation Frequency})$$

2-60. Phase modulation is programmed normalized to 10 kHz modulation frequency. This means that phase modulation is processed internally just as FM after multiplying the phase modulation index by 10 kHz to get the equivalent FM deviation.

2-61. The operator can control the angle modulation through a front panel button entry, IEEE-488 bus command, edit knob operation, or through an external signal applied to a front panel connector.

2-62. The amount of peak deviation allowed depends upon the frequency range and whether or not the center frequency is unlocked (DCFM Mode).

2-63. Programming of angle modulation is inseparable from programming of frequency modulation. The calculation of frequency and deviation parameters is handled so as to avoid conflict. Programming angle modulation uses the programmed frequency to calculate the deviation range referred to the fundamental frequency band. But programming frequency can change the deviation range which in turn determines whether or not the HI DEV mode is enabled. To avoid this fatal conflict, angle modulation is programmed in line with the frequency programming path. This means that every time angle deviation is programmed, frequency is programmed, and every time frequency is changed, angle modulation is reprogrammed, but only if angle modulation is enabled.

2-64. Since angle modulation is implemented in the synthesizer section (in the 250-MHz to 520-MHz band), the required FM depth DAC settings, FM range, and scale factor are calculated by referring the desired FM output deviation to the fundamental (250 MHz to 520 MHz) band. Tables 2-3, 2-4, and 2-5 show the FM DAC full scale, RF multiplier, FM range, and scale factor for normal (autoranging), HI DEV, and DCFM modes. The product of these four values equals the output FM full scale deviation. After obtaining these values the microprocessor calculates the FM depth DAC value as a proportion of the desired deviation to the full scale deviation. Next the processor determines whether the HI DEV mode is required (if deviation referred to the fundamental band exceeds 199 kHz.)

2-65. GENERATOR OUTPUT VALID STATUS

2-66. The output valid status is available at a rear panel connector labeled OUT VALID and also through the IEEE interface. The output valid status indicates unsettled transient conditions where the output of the instrument is impaired or unusable. It can be used to synchronize IEEE programming of the instrument with the settling of the output as a result of a previous change.

2-67. The output valid signal is a combination of hardware and software conditions. Output valid is false during the following periods of time:

1. For 50 ms after HI DEV mode is asserted.

2. From the time HI DEV is disabled until 5 ms after DDNR (Delay Discriminator Not Ready) becomes false.

3. From the time frequency is programmed when not in HI DEV mode until 5 ms after DDNR becomes false.

4. From the time frequency is programmed in the HI DEV mode until 50 ms after the frequency control data is transferred to the N/1 Divider (N1TST goes negative at the time transfer is initiated).

5. For (200 + (kHz DEV RGE)/10) ms after enabling FM.

6. For ((kHz DEV RGE)/10) ms after ranging FM, once enabled.

7. For 50/FM ms after enabling MOD OSC or ranging, once enabled (FM in kHz).

8. For 150 ms after DCFM is enabled.

2-68. INSTRUMENT SELF-TEST

2-69. The 6070A and 6071A provide extensive self-checking capabilites of their digital and analog hardware. Instrument self-tests are activated automatically at each power-on and can also be activated by selecting special function 02.

Table 2-3. FM Range (and Scale Factor) for the Normal Mode

Output FM Dev FS (kHz)		1000	500	200	100	50	20	10	5
Output ϕ Index FS (RAD)		100	50	20	10	5	2	1	0.5
FM DAC FS		1000	1000	800	1000	1000	800	1000	1000
BAND (MHz)	RF MULT.								
520-1040	2	1/2 (1)	1/4 (1)	1/10 (5/4)	1/20 (1)	1/40 (1)	1/100 (5/4)	1/100 (5/4)	1/100 (5/4)
250-520	1	1 (1)	1/2 (1)	1/4 (1)	1/10 (1)	1/20 (1)	1/40 (1)	1/100 (1)	1/100 (1)
125-250	1/2	1 (1)	1 (1)	1/2 (1)	1/4 (4/5)	1/10 (1)	1/20 (1)	1/40 (4/5)	1/100 (1)
62.5-125	1/4	1 (1)	1 (1)	1 (1)	1/2 (4/5)	1/4 (4/5)	1/10 (1)	1/20 (4/5)	1/40 (4/5)
0.2-62.5	1	1 (1)	1/2 (1)	1/4 (1)	1/10 (1)	1/20 (1)	1/40 (1)	1/100 (1)	1/100 (1)

Table 2-4. FM Range (and Scale Factor) for the HI Dev Mode

Output FM Dev FS (kHz)		1000	500	200	100	50	20	10	5
Output ϕ Index FS (RAD)		100	50	20	10	5	2	1	0.5
FM DAC FS		1000	1000	800	1000	1000	800	1000	1000
BAND (MHz)	RF MULT.								
520-1040	2	1/2 (1)	1/4 (1)	1/10 (5/4)	1/20 (1)	1/20 (1)	1/20 (1)	1/20 (1)	1/20 (1)
250-520	1	1 (1)	1/2 (1)	1/4 (1)	1/20 (1)	1/20 (1)	1/20 (1)	1/20 (1)	1/20 (1)
125-250	1/2	1 (1)	1 (1)	1/2 (1)	1/4 (4/5)	1/10 (1)	1/20 (1)	1/20 (1)	1/20 (1)
62.5-125	1/4	1 (1)	1 (1)	1 (1)	1/2 (4/5)	1/4 (4/5)	1/10 (1)	1/20 (4/5)	1/20 (4/5)
0.2-62.5	1	1 (1)	1/2 (1)	1/4 (1)	1/10 (1)	1/20 (1)	1/20 (1)	1/20 (1)	1/20 (1)

Table 2-5. FM Range (and Scale Factor) for the DCFM Mode

Output FM Dev FS (kHz)		1000	500	200	100	50	20	10	5
Output ϕ Index FS (RAD)		100	50	20	10	5	2	1	0.5
FM DAC FS		1000	1000	800	1000	1000	800	1000	1000
BAND (MHz)	RF MULT.								
520-1040	2	1/2 (1)	1/4 (1)	1/10 (5/4)	1/20 (1)	1/40 (1)	1/100 (5/4)	1/100 (5/4)	1/100 (5/4)
250-520	1	1/2 (1)	1/2 (1)	1/4 (1)	1/10 (1)	1/20 (1)	1/40 (1)	1/100 (1)	1/100 (1)
125-250	1/2	1/2 (1)	1/2 (1)	1/2 (1)	1/4 (4/5)	1/10 (1)	1/20 (1)	1/40 (4/5)	1/100 (1)
62.5-125	1/4	1/2 (4/5)	1/2 (4/5)	1/2 (4/5)	1/2 (4/5)	1/4 (4/5)	1/10 (1)	1/20 (4/5)	1/40 (4/5)
0.2-62.5	1	1/2 (1)	1/2 (1)	1/2 (1)	1/2 (1)	1/2 (1)	1/40 (1)	1/10 (1)	1/20 (1)

2-70. At power-on the instrument processor checks the program ROM checksum and the scratch pad RAM. After these two checks have been performed, the instrument can be programmed through the front panel. The instrument can be programmed through the IEEE compatible interface after all of the self-tests are complete. The following tests are performed after the ROM and RAM self-tests are completed. The test sequence is terminated immediately if any front panel button is pushed.

1. The calibration PROM checksum.

2. The IEEE circuitry is tested by writing data to the IEEE chip (U39) and verifying the data by reading it back.

3. If the nonvolatile memory is installed, each register of the nonvolatile RAM is checked with a checksum.

4. The low pass filters in the modulator/divider board are tested by setting the frequency above the cutoff and checking the unleveled indicator. This procedure checks portions of the modulator/divider, output amplifier, phase detector, N/1 divider, single sideband mizer, VCO, sub-synthesizer, and 10 MHz reference.

5. The delay discriminator is tested by stepping the frequency and then checking the delay discriminator not ready indication (Self-Test Error Code). This procedure also checks portions of the phase detector, N/1 divider, single sideband mixer, sub synthesizer, and 1-MHz reference.

6. Loopback test bits on the N/1 divider, sub-synthesizer and modulator distribution boards are checked. The loopback test bits can be both written to and read by the CPU. The processor sets these bits and then reads back the value to check that they are operating correctly. This checks portions of the cable between the CPU and the synthesizer output modules as well as the N/1 divider, sub-synthesizer, and modulation distribution printed circuit boards.

7. If the instrument is a 6071A the output amplifier is tested by programming the frequency in each of the X2 bands and verifying that the instrument is still leveled at 1 dB above the calibrated level.

8. The sub-synthesizer unlock indicator is checked by forcing a change in frequency. When this is done, the sub-synthesizer should lock again within 100 ms. This procedure also checks a portion of the 10 MHz reference.

9. Frequency modulation is checked by overmodulating the carrier and then by checking the reduce peak deviation (Error Code Indication). This checks portions of the modulation oscillator, the modulation distribution pcb, the phase detector, the N/1 divider, the single sideband mixer,

the VCO, the sub-synthesizer, and the 10 MHz reference.

10. Amplitude modulation is checked by overmodulating the carrier and then by checking the unleveled indicator. This procedure also checks portions of the modulation oscillator, modulation destribution logic, output amplifier, modulator/divider, phase detector, N/1 divider, single side band mixer, VCO, sub-synthesizer, and 10 MHz reference.

11. The Front panel buttons aren't checked at power on, but the operator can check permanently open buttons by performing special function 04. When special function 04 is invoked, each button pushed will have its row and column address displayed in the center of the frequency display field. The special function is exited by pushing the CLEAR button. Refer to the FrontPanel Control Check in the Calibration Manual.

12. The front panel displays and LEDS are not checked at power on, but can be checked any time by performing special function 03. When this is done, the microprocessor cycles through all display segments and LEDs twice. This checks for shorts between column lines and shorts between row lines. Refer to Front Panel Control Check in the Calibration Manual.

13. If one or more of the tests failed, the results of the failed test are displayed (see Section 5E of the 6070A/6071A Operator Manual).

14. The instrument then assumes its power-on status.

2-71. Self-check errors are displayed in the amplitude display field during power-on instrument identification. If the instrument fails one or more of the self-tests, the instrument model number (6070A or 6071A) appears in the FREQUENCY display and an error code indicating the test(s) failed appears in the AMPLITUDE display. For a list of error codes and interpretations refer to the Self-Test Error Code Interpretations Table in Section 5E of the 6070A/6071A Calibration Manual.

2-72. POWER-ON SETTING WITHOUT NON-VOLATILE MEMORY OPTION

2-73. When the 6070A or 6971A POWER control is set to ON, the instrument automatically sequences through a series of self tests and displays. After approximately five seconds, the front panel is set up to the programmed power-on setup unless the instrument failed one or more of the self tests. For a listing of the instrument's power-on setup, refer to Section 5 in the 6070A/6071A Calibration Manual.

2-74. POWER-ON SETTING WITH NON-VOLATILE MEMORY OPTION

2-75. If the instrument has the 6070A-570 Nonvolatile Memory Option installed the front panel is returned to the last setup before the instrument was placed in standby. If the last setup included sweep, sweep will be turned off.

2-76. INSTRUMENT IDENTIFICATION, SOFTWARE REVISION NUMBER, AND SELF TEST RESULT

2-77. The instrument identification, software revision number, and self-test codes are displayed on the front panel when the operator selects special function 09. The same codes, excluding the software revision number are also displayed after the power-on self test if one or more of the self tests failed. Refer to Section 5E of the 6070A/6071A Operator Manual for theSelf-Test Error Code Interpretation Table.

2-78. INTERROGATE STATUS RESPONSE FORMAT

2-79. In response to an INTERROGATE command, the front panel display field displays either the UNCAL (uncalibrated) condition codes or the REJ ENT (rejected entry) condition codes depending on whether the UNCAL status or the REF ENT annunciator is lit. For a complete description, refer to the Interrogate Operation material in Section 5E of the 6070A/6071A Operator Manual.

2-80. INTERROGATE REJECTED ENTRY STATUS FORMAT

2-81. When the operator makes an illegal entry, the REJ ENT annunciator flashes. For a complete description, refer to the Interrogate Operation paragraph in Section 5E of the 6070A/6071A Operator Manual.

2-82. THEORY OF OPERATION

2-83. Introduction

2-84. The Fluke Models 6070A and 6071A are fully electronically tuned and operated solid-state general-purpose signal generators. They each employ a coaxial cable delay line descriminator for spectral noise suppression and a microprocessor for all local and remote control function as well as for level correction and FM accuracy enhancement. The two generators are identical except for the output amplifier module. The 6070A, which has an upper frequency limit of 520 MHz, uses the A4A7 Output Amplifier. The 6071A, which has an upper frequency limit of 1040 MHz, uses the A4A6 X2 Output Amplifier.

2-85. Physical Layout

2-86. INTRODUCTION

2-87. Physically, the instrument consists of five modules: the front panel, the rear panel, the synthesizer module, the output module, and the delay line module.

2-88. THE FRONT PANEL

2-89. The front section includes the A1A1 Front Panel PCB, the A2A1 Controller PCB, and the optional A2A2 Nonvolatile Memory PCB. The front panel provides the interface between the operator and the signal generator's functional hardware. A 16-bit microprocessor (TMS9900), in conjunction with the software instructions, acts upon the operator commands, whether via the front panel or the IEEE interface, to configure the circuitry and apply corrections. In addition the microprocessor alerts the user of various conditions which may impair the output signal.

2-90. THE REAR PANEL

2-91. The rear panel contains the power supply and the cooling fan. The power supply consists of a high efficiency switching supply followed by series-pass regulators to provide +5V, -12V, +12V, and +24 volts. The switching supply is housed in a shielded enclosure that suppresses radiation and leakage.

2-92. THE SYNTHESIZER AND DELAY LINE MODULES

2-93. The synthesizer and delay line sections provide the frequency generation and angle modulation functions of the instrument. Physically the synthesizer section is the upper swing-out module located in the middle of the instrument. The main phase-locked loop located in this section consists of the A3A5 VCO PCB, the A3A6 SSB Mixer PCB, the A3A4 N/1 Divider PCB, and the A3A1 Phase Detector PCB. The reference signal for the phase detector is supplied by the A3A2 10-MHz Reference PCB. The main loop generates frequencies in the 250-MHz to 520-MHz band with 100 kHz resolution. Additional resolution (1 Hz below 520 MHz to 2 Hz above) is provided by the A3A7 Sub-Synthesizer PCB. The FM noise of the main-loop A3A5 VCO is suppressed by a negative-feedback control system in which the A3A3 Delay Discriminator PCB and the Delay line (A7), function as an FM demodulator. Two other printed circuit boards, the A3A8 Synthesizer Control Buffer and the A3A9 Synthesizer Distribution, provide the digital control interface between the synthesizer module and the controller.

2-94. THE OUTPUT MODULE

2-95. The output section is the lower swing-out module and contains the level control, amplitude modulation, RF bandswitching, audio processing, and the output protection functions. The following printed circuit boards are located in this section: the A4A4 Modulator Divider, the A4A8 Heterodyne Oscillator, the A4A9 Hetrodyne Converter, the optional A4A5 Reverse Power Protector, the A4A2 Modulation Oscillator, the A4A10 Modulation Distribution Assembly, and the A4A7 Output Amplifier for the 6070A or the A4A6 X2 Output Amplifier for the 6071A, and the A4A3 Attenuator.

2-96. Frequency Bands

2-97. The frequency coverage is derived from a fundamental 250-MHz to 520-MHz phase-locked oscillator which is subsequently frequency-divided by two or four, or heterodyned, or in the case of the 6071A, multiplied by two. The fundamental band and the two divided bands each employ two half-octave switched low-pass filters to suppress harmonics. The doubled band uses four switched quarter octave bandpass filters to suppress harmonics and sub-harmonics. The 0.2-MHz to 62.5-MHz heterodyne band is generated by mixing a portion of the fundamental band with a fixed 520-MHz signal from a surface-acoustic-wave (SAW) oscillator. All of the band switching is done automatically, under microprocessor control so it is not apparent to the user. On the fundamental, divided, and hetrodyned bands, seven modulators provide the bandswitching as well as amplitude modulation (AM) and level control.

2-98. Level Control

2-99. A 6 dB per step attenuator (A4A3) and a switched 6 dB gain amplifier maintain coarse control of the output level. Fine control of the output is accomplished by means of a vernier level DAC (A4A10U29) which varies the automatic level control (ALC) loop reference. Control of the step attenuator/amplifier and the vernier DAC is orchestrated automatically by the microprocessor. In addition, the microprocessor applies level correction (a linear function of frequency between calibration frequencies) to compensate for the frequency response of the 6-dB amplifier or the attenuator section(s) in use. This microprocessor correction is applied only to the vernier level DAC; it does not affect the level at which the step attenuator or 6-dB amplifier switches. In other words, all generators will have the same attenuation switched in at a particular programmed level, even though the correction factor is different from synthesizer to synthesizer.

2-100. Frequency Synthesis

2-101. The main phase-locked loop (PLL), which synthesizes the fundamental frequency (250 MHz to 520 MHz band), is a modified divide-by-N loop with a mixer in the feedback path. The reference frequency for the loop is 2 MHz, which would normally provide 2 MHz steps in a conventional divide-by-N loop. However, this instrument uses a modified divide-by-N circuit involving a pulse-deletion function controlled by a rate multiplier to provide 0.1 MHz steps. Additional resolution is gained by a signal from the sub-synthesizer which is introduced into the main loop via the single sideband mixer in the feedback path and provides frequency steps of 1 Hz. The sub-synthesizer loop is similar to the main loop in that it also uses a pulse-deletion function and a single sideband mixer for additional resolution.

2-102. The controller takes into account the frequency dividing, multiplying, or inverting action (on the heterodyne band) of the various bands as well as the offset

introduced by the mixers in the two loops. Also, since the main PLL bandwidth varies with the programmed frequency (due to N changing and variations in the VCO coefficient), the controller programs the phase detector gain in a compensating manner to maintain constant loop bandwidth. By keeping the loop bandwidth constant, loop stability is assured and the modulation transfer response of the loop is controlled so that accurate, high-rate FM is possible.

2-103. Angle Modulation

2-104. Frequency modulation (FM) is implemented by applying the modulation signal simultaneously to the main PLL VCO and Phase Detector, because the main-loop bandwidth is approximately 1 kHz (which is within the modulation frequency range). The loop's response to a modulating signal is frequency modulation with a frequency response like a high-pass filter for signals introduced at the VCO, and phase modulation with a frequency response like a low-pass filter for signals introduced at the phase detector. By pre-processing the modulating signals with an integrator, the phase modulation characteristics for the signal introduced at the phase detector can be made to look like frequency modulation. Then, applying the unprocessed signal to the VCO results in a flat overall FM response. Because the modulation introduced at the phase detector is effectively multiplied by N (where N is the main loop divider ratio) this effect is compensated by scaling the modulating signal. This scaling is done by a multiplying DAC (A4A10U12). Likewise, the modulating signal applied to the VCO is adjusted in amplitude by a multiplying DAC (A4A10U25) to compensate for variations in the VCO tuning. This is done automatically by the controller using measured data which is stored in the calibration EPROM (A2A1U11).

2-105. Phase modulation (ϕM) is similar to FM except the modulating signal is preprocessed in the opposite manner (i.e., the signal applied to the phase detector is unprocessed, and the signal applied to the VCO is differentiated). The integrator or differentiator is enabled automatically by the controller when FM or ϕM is selected. The controller also calculates the FM range and deviation referred to the fundamental band and programs the hardware accordingly. The ϕM is programmed normalized to 10-kHz modulating frequency. This means that ϕM is processed internally just as FM after multiplying the ϕM index by 10 kHz to get the equivalent FM deviation.

2-106. DCFM

2-107. On the 0.2 to 62.5 MHz band, DCFM is generated by frequency modulating directly (and only) the A4A8 Heterodyne Oscillator. When the modulated Heterdyne Oscillator signal at 520 MHz is mixed with the main-loop synthesized signal, the frequency modulation is transferred to the generator's output. On the other bands, the Heterodyne Oscillator is not used directly to generate the output frequency, but instead it is used to provide a DC frequency modulated reference signal to the main loop. However, frequency modulation introduced in this manner only works for modulation frequencies up to the loop bandwidth due to the low-pass nature of the loop. Therefore, the modulating signal is simultaneously applied to the main loop A3A5 VCO to provide an overall flat modulation response.

2-108. DETAILED CIRCUIT ANAYSIS

2-109. Introduction

2-110. The following paragraphs describe, in detail, the more complex circuits in the synthesizers.

2-111. A1A1 Front Panel PCB and A1A2 Encoder Optic PCB Circuit Analysis

2-112. INTRODUCTION

2-113. Refer to the System Block Diagram and the A1A1, A1A2 Front Panel PCB Schematic in the 6070A/6071A Schematic Manual. The A1A1 Front Panel PCB is located in back of the 6070A/6071A front panel. The A1A2 Encoder Optic PCB is part of the Encoder Assembly.

2-114. ENCODER CIRCUIT ANALYSIS

2-115. The knob rotation is sensed by two LED/phototransistor optical switches located on the A1A2 Encoder Optic PCB. The switches are positioned to give a quadrature phase output when the knob is turned. In the rest position DT2 is centered on a tooth of the encoder disc giving a TTL low at TP2 (window), and DT1 is on the edge of a tooth allowing TP1 (trigger) to be high or low. U25 is a quad Schmitt trigger NAND gate; two of the gates are used to provide noise immunity and buffering. Quad NAND gate U22 isconfigured so that either a positive-or negative-going edge provides a pulse with a duration of four gate delays. NAND gate U24-3 combines the edge detector pulses and U24-10 only gates the pulses when TP2 is high. NAND gate U24-11 provides the clock pulses to latch both the direction and interrupt status for the processor. When the knob interrupt is serviced, U21-5 is then preset by the microprocessor.

2-116. The only user adjustment on the A1A2 Encoder Optic PCB is the magnetic detent gap, which is set by positioning the clearance between the pole and teeth to 0.000 inches and then turning the screw clockwise 1/4 turn to 1/2 turn (a gap of 0.002 to 0.003 inches).

2-117. SWEEP OUTPUT

2-118. A microprocessor controlled 0 to 10 volt output is provided that is proportional to the output frequency when sweeping between a start and stop frequency. The digital to analog converter (DAC) is comprised of a current DAC (U34) and an operational amplifier (U33). Resistor R40 is in series with the DAC output to provid short-circuit protection.

2-119. MULTIPLEXED DISPLAYS AND KEYBOARD

2-120. The display is updated approximately every one millisecond for each of the 10 digits and the bright digit is updated for approximately four milliseconds; therefore, a complete display update takes about 14 milliseconds. Flip-flop U20 is used to clear the displays if a new digit is not latched. This protects the displays if the microprocessor should stop refreshing. The same control lines that select the display digits are used to enable the keyboard column selects. The rows are then multiplexed by U23 and read by the microprocessor. Since each column must be stobed, it takes about 14 milliseconds for the keyboard to be read. Potentiometer R30 adjusts the front panel MOD OUT signal from the A4A2 Modulator Oscillator PCB. Switch S1 is the front panel POWER ON/STBY switch.

2-121. A2A1 Controller PCB Circuit Analysis

2-122. INTRODUCTION

2-123. Refer to the System Block Diagram and the A2A1 Controller Schematic located in the 6070A/6071A Schematic Manual.

2-124. MICROPROCESSOR

2-125. A 16-bit microprocessor U22 (TMS9900) is used to control the 6070A and 6071A Synthesized RF Signal Generators. The microprocessor requires ground and threee supply voltages: +5V dc (VCC), +12V dc (VDD), and -12V dc (VBB).

2-126. CLOCK GENERATOR

2-127. The microprocessor U22 requires a four-phase clock which is provided by clock generator U25 (TMS 9904). Capacitor C19 sets the oscillator frequency. C20 and L3 select the third overtone.

2-128. RESET

2-129. The clock generator also has an internal flip-flop which is used for the reset signal. The input originates from comparator U53 and is used to monitor the +5-volt supply referenced against the +12 volt supply. The output of this internal flip-slop is then used as the reset signal to the microprocessor and to U26. This insures that the clock signals are correct before the microprocessor reset signal is removed. A reset signal for the nonvolatile RAM is formed by anding the comparator output and the flip-flop output in CR9 and CR10 so that the reset signal to the RAM is in a defined state when power is switched on and off. When the 5V power supply is at 5 volts, CR7 will be lit.

2-130. INTERRUPTS AND CONTROL/STATUS

2-131. The programmable systems interface U26 (TMS 9901) is used to handle the system interrupt lines and the control and status lines which are used most often. There are three interrupt lines: the IEEE-488 interrupt line, the front panel edit knob interrupt line, and the timer interrupt line (part of U26 used for timing keyboard inputs, display refreshing, and flashing annunciators). The remaining input/output lines used are buffered by U27, U28, and U31 and are decoded on the A1A1 Front Panel PCB, A4A10 Modulation Distribution PCB, and A43A9 Synthesizer Distribution PCB. U34 and U35 form a one-of-eight decoder which performs input/output decoding.

2-132. RAM/EPROM

2-133. The microprocessor needs RAMs (U1 through U4) and EPROMs (U7 through U15). The RAM and EPROM select lines are decoded by a one-of-eight decoder (U16). The RAMs are used as general purpose registers and ordinary read/write memory. The EPROMs (excluding U11) contain the microprocessor instructions and costant data. The Calibration EPROM (U11) contains calibration data which is specific to a synthesizer.

2-134. IEEE-488

2-135. The IEEE-488 compatible bus is controlled through U39 (MC 68488), which interfaces to the microprocessor through synchronizing circuitry. NAND gate U42-6 detects a write condition (DBIN), which enables U43-6 to gate out the microprocessor select signal (MS) from decoder U16 on a read or a write for addresses (AB12 through AB14). This gated chip select signal (MS) is then gated again by U43-3 which is controlled from U42-3. (U42-3 is enabled if U39 had been previously disabled.) When the phase 1 clock goes low (from U46 pin 5 to U42 pin 2), the READY line goes low. The microprocessor then forces WAIT high and allows U39 to be selected. Flip-flop U47-6 and NOR gate U37-6 produce a square wave enable signal at U39 if R/W (U39 pin 5) is low (a write sequence), or a non symmetrical wave if R/W is high (a read sequence).

2-136. Integrated circuit U33 is a tri-state buffer used to read the IEEE-488 bus address switches. Integrated circuit U44 is also a tri-state buffer which is used to switch the data direction on the IEEE-488 bus. Drivers U41, U45, U50, and U51 connect directly to the IEEE-488 bus.

2-137. TEMPERATURE SENSOR

2-138. An over-temperature detector (RT1, U52, and Q1) forces the instrument into a standby condition if the CPU temperature exceeds 65 degrees Celsius (149 degrees Fahrenheit). If this occurs, the fan remains on.

2-139. KERNAL TEST

2-140. The microprocessor and clock generator may be tested by removing U16, U17, U18, and the optional nonvolatile RAM (located on A2A2 PCB) and by setting switch U30-1 to the on (closed) position. This will cause a square wave output on the 15-bit address bus (U22 pins 10 through 24), with the frequency doubling with each address line. The square wave on AB14 will be the lowest

frequency, the square wave AB13 will be double that on AB14, the square wave on AB12 will be double that on AB13 etc., up to AB0 which will be the highest frequency. Most of the IEEE-488 bus synchronizing circuitry may be checked by replacing U16. This will cause a nonsymmetrical output on U22 (pin 10 through pin 24) when the IEEE-488 bus is addressed. Switch U30-2 should normally be in the off (open) position. When switched to the on (closed) position, the self-tests performed on power-on will be skipped. Switches U30-3 and U30-4 should always be in the off (open) position.

2-141. A2A2 Non-volatile Memory PCB Circuit Analysis (Option 570)

2-142. Refer to the System Block Diagram and the A2A2 Nonvolatile Memory PCB schematic located in the 6070A/6071A Schematic Manual.

2-143. The A2A2 Nonvolatile Memory PCB (Option 570) stores up to 50 front panel setups. These setups are retained when the 6070A/6071A is in the standby mode or when the instrument is disconnected from main power. This is accomplished by using CMOS RAMs (U14 to U29) to store the setups and a lithium battery (BAT 1) for backup power when disconnected from the main power. The battery provides more than two years of memory retention with no main power. When switch S1 is open the battery is out of the circuit. When switch S1 is closed the battery is in the circuit.

2-144. There are three sources of power for the RAMs: the battery, the standby supply, and the regulated 5-volt source for the operating mode. A series-pass regulator (Q1, Q2, U30) ensures that the CMOS RAMs operate at the same voltage as the support circuitry. Thus, the regulated +5 volt supply prevents the CMOS RAMs from latching up. Diodes CR1 and CR5 pass current from Q1. The regulator works by CR5 drawing from the same current that the CMOS RAMs draw through CR1. Any change in voltage from comparator U30-7 is applied to the base of Q1. The current is then adjusted through Q1 so that the anode of CR5 is maintained at +5 volts which is the same level as the +5 volt supply to the CMOS RAMs (VCCDR).

2-145. The presence of the nonvolatile memory option is automatically detected by the microprocessor when J2 is plugged into the controller board (A2A1). The signal NVOPL is pulled up to +5 volts when the option is not installed and pulled to ground when J2 is plugged in.

2-146. The RAM chips are decoded by the one-to-eight decoder U5. Eight-bit, single directional bus drivers are used on the low order address bus (U4) and on the data bus (U6 through U9). The data bus drivers are enabled only when the microprocessor memory enable signal (MEMEN) from the microprocessor is low and AB14, AB13, and AB12 are 1, 1, and 0, respectively. The microprocessor signal DBIN is used to determine the direction of the data flow by enabling U6 and U8 for a read from RAM and by enabling U7 and U9 for a write to RAM.

2-147. A3A1 Phase Detector PCB Circuit Analysis

2-148. Refer to the System Block Diagram and the A3A1 Phase Detector Schematic located in the 6070A/6071A Schematic Manual.

2-149. The A3A1 Phase Detector PCB provides the control voltage to the A3A5 VCO or the A3A3 Discriminator stabilized VCO, to keep the loop locked to the appropriate reference with the necessary spur and noise performance. The A3A1 Phase Detector is also involved in processing some of the FM modulation.

2-150. The 10 MHz reference either from a crystal oscillator via the A3A2 10 MHz Reference PCB (J1-PD10M) or from the A4A8 Het Oscillator PCB (J3-VAR10M) is selected by U1 and the VAR10L control line. The ECL signal from the DCFM oscillator is transformed to TTL by circuitry associated with Q1 and Q2. When the DCFM mode and RF frequencies below 62.5 MHz are selected, then VAR10L is asserted (low) turning on Q9 which provides the proper ECL termination conditions with R19 and R53. Transistors Q1 and Q2 switch the current supplied by R15 into ground or into R20. Resistors R16 and R17 provide bias for Q2. The 10 MHz TTL signal from Q2 passes through U1 to a 5:1 divider, U2. When VARI0L is high, the fixed 10-MHz signal is coupled to the divider, Q9 is turned off, and the ECL termination becomes +5V, which turns the signal off.

2-151. The 2 MHz reference signal from the 5:1 divider U2 and the 2 MHz signal from the A3A4 N/1 PCB (J4-2 MHz) are connected to a digital phase-frequence detector (U3 and U4). If the frequency of the signal from the A3A4 N/1 PCB is greater than the reference frequency, there will be positive going pulses at TP5. When TP5 is above ground potential, CR5 is off and CR6 allows the down current from Q6 to flow into the integrator U5. This decreases the voltage at TP6 which lowers the VCO frequency and causes the loop to lock. Test point TP7 is kept positive which allows the up current from R46 to flow out of Q4 instead of the integrator. Similarly, if the N/1 output frequency is below the reference frequency, there wil be negative-going pulses at TP7. When TP7 potential is below ground, CR8 is off and CR7 allows the up current to flow out of the integrator through R46. This increases the voltage at TP6 which raises the VCO frequency. Test point TP5 is kept negative which allows the down current from Q6 to flow into R32 instead of the integrator. Level shifters (Q3, Q4, R22, R23, R24, R32, R33, and R34) center the TTL swing approximately at ground.

2-152. The voltage-to-current converter (Q5, Q6, R42, R44, and U12) supplies the up current by mirroring the current across R45. The voltage at U12-2 is held close to ground so the current produced is proportional to the KVN voltage (P1-13, TP8). The voltage, which is generated by a DAC on the A3A8 Synthesizer Control Buffer PCB, is controlled by the microprocessor. By changing the phase detector current, which changes the pase detector gain (Kϕ in volts/radian), the phase-locked loop bandwidth can be kept constant. A small amount of leak current is pulled out of the integrator by R47 to bias the phase detector at about 2 radians. Under normal operation there should be 2 MHz 200 nS pulses at TP5, and TP7 should be positive. If the loop unlocks there would be pulses at TP7 and, consequently, at C36, C37, R21, R41, and U11. The output of the one-shot produces an error flag (RPDH, P1-12) which is periodically polled by the microprocessor.

2-153. The integrator consists of low-noise operational amplifier U5, C26, R25, and R26. Capacitators C23 and C30 provide some filtering of the 2 MHz reference energy. The output of the operational amplifier is connected, via a test switch SW1, to a multi-pole LC filter (C24, C25, C28, C29, C33, L4, L5, R28, and R31) which attentuates the delete rate (n*100 kHz) and reference (2 MHz) spurs. Diode speed-up networks (CR1, CR2, CR3, CT4, R27, and R29) reduce the source impedance to improve switching speed. Switch SW1 shorts the integrating capacitor C26 and allows the VCO to be tuned by a limited variability dc voltage (from R36, R37, and R38) which puts the output frequency at approximately 375 MHz. The switch is useful for breaking the loop when troubleshooting.

2-154. The FM audio signal (PD FM, P1-11), from the KV DAC on the A3A9 Synthesizer Distribution PCB, is split into two paths on the A3A1 Phase Detector PCB. The path which connects to the integrator U5 is for modulation frequencies inside the phase-locked loop bandwidth. The path which connects to the A3A3 Delay Discriminator PCB (DIFM, P2-1) is for modulation frequencies outside the phase-locked loop bandwidth. The phase-locked loop bandwidth is approximately 800 Hz in the discriminator mode (HI DEV off) and 2 kHz in the high deviation mode (HI DEV on).

2-155. A compensation network (C1, C2, C3, C4, C7, U17, and U18) corrects for the effect of the cleanup loop that follows the signal sideband mixer in the feedback path of the main phase-locked loop. Resistors R1, R2, and R50 provide offset voltage compensation. Resistor network U16 in conjunction with DMOS switches (U14 and U15) are for FM range switching, (Table 2-6).

2-156. Comparators U7 and U8, along with pull-up U10, level shift TTL to the ±12V necessary to operate the DMOS switches. U9 is a 3-to-8 line decoder. Operational amplifier U13 operates as an integrator (to convert ϕ/M to FM) in the FM mode or as an amplifier in the ϕM mode. The audio integrating capacitor C15 is switched by K1. Resistor R11 provides DC stability. A portion of U14 is used to switch in a fixed resistor R9 in the ϕ/M mode. Capacitor C14 provides bandwidth limiting in the ϕ/M mode. The audio signal is AC coupled to the phase detector integrator U5 via C12, C13, Q7, R10, R13 in the FM mode. (Resistor R10 adjusts the low frequency FM gain.) The audio signal is DC coupled to the phase detector via Q8, R12, and R14 in the ϕM mode. Resistor R12 adjusts the low frequency ϕ/M gain. FET's Q7, and Q8 are switched by U7, CR10, and CR11. Resistor R35 is used for offset voltage compensation.

2-157. The high frequency audio is processed by circuitry associated with U20. In the FM mode, U20 is an amplifier whose gain is set by R4 AND R7.Resistor R5 adjusts the high frequency FM/OM balance, and R4 adjusts the overall high frequency gain. In the O/M mode, U20 is a differentiator. The differentiation bandwidth is set by C8 and R3. The two modes are switched by U19 in conjunction with U6 (PHMODL, P1-6). Capacitor C11 provides stability for U20.

2-158. A3A2 10 MHz Reference PCB Circuit Analysis

2-159. BRIEF DESCRIPTION

2-160. Refer to the System Block Diagram and the A3A2 10 MHz Reference PCB schematic located in the 6070A/6071A Schematic Manual for the following Circuit Analysis. Figure 2-1 is a block diagram of the A3A2 10-MHz Reference PCB.

2-161. The A3A2 10-MHz Reference PCB generates the 10 MHz reference signal for the Models 6070A and 6071A RF Synthesized Signal Generators. The 10-MHz signal is generated locally on the pcb in a non-temperature controlled crystal oscillator or off the pcb in an optional 607XA-130 Oven Reference Oscillator. However, an external reference signal can also be used. The selection between internal crystal oscillator and external input is done automatically whenever an external signal is applied. There are two modes of external input operation:

Table 2-6. FM Range Switching

FM RANGE	CONTROL LINE	CONTROL PDRN (2,1,0)H
1 MHz*	7	111
500 kHz*	6	110
200 kHz	5	101
100 kHz	4	100
50 kHz	3	011
20 kHz**	2	010
10 kHz**	1	001

*Used only in the high deviation mode (HI DEV on)
**Used only in discriminator mode (HI DEV off)

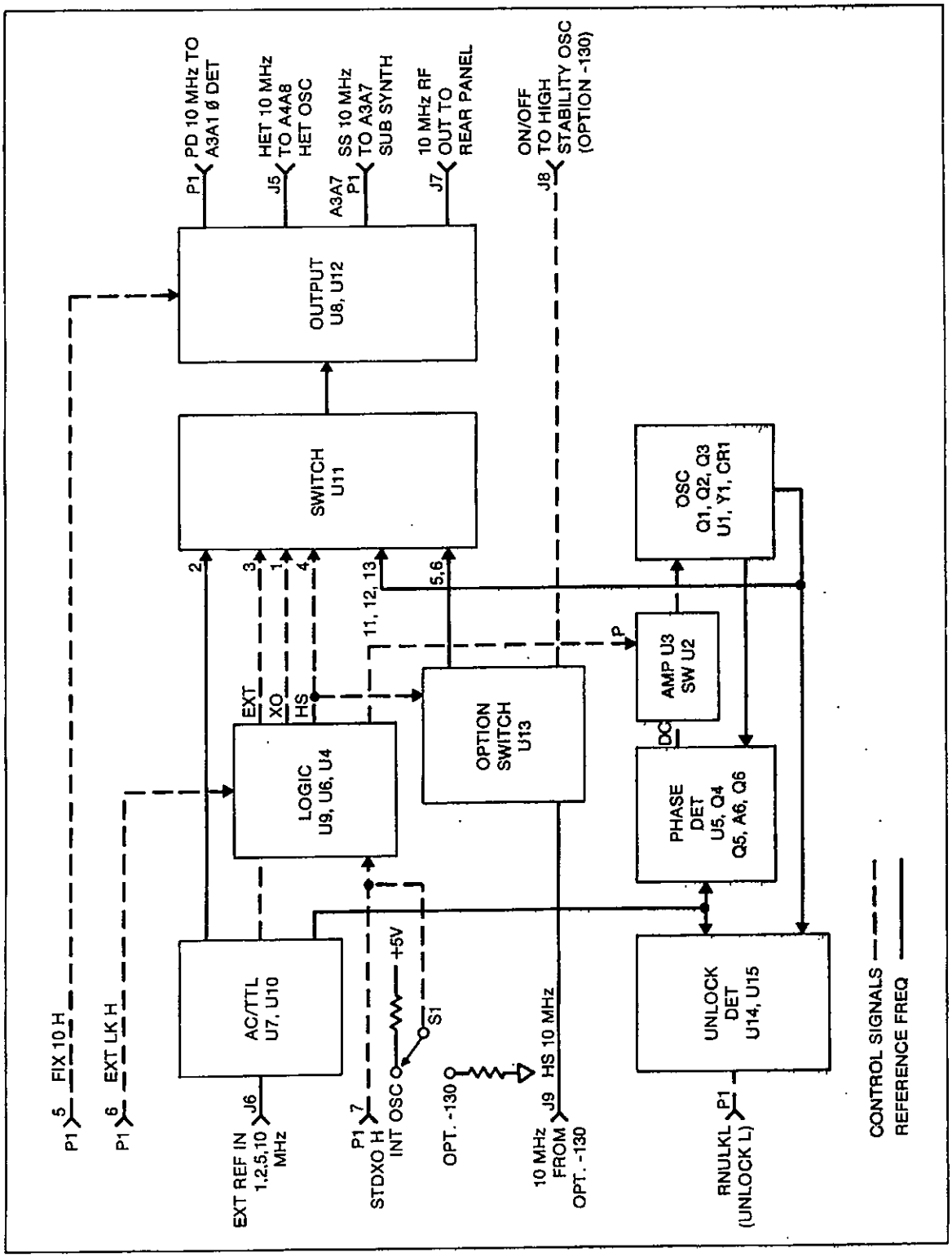

Figure 2-1. A3A2 10 MHz Reference PCB Block Diagram

1. The A3A2 10 MHz Reference PCB crystal oscillator is locked to a 10 MHz reference signal or a subharmonic of 10 MHz (limited lock range). This mode uses the pcb crystal oscillator even with the 607XA-130 Oven Reference Oscillator option.

2. An external 10-MHz reference signal is used directly. This is called the wideband mode.

2-162. The A3A2 10-MHz Reference PCB supplies signals and control for the following:

1. A3A1 Phase Detector PCB (phase detector, main loop, 10 MHz).

2. A4A8 Heterodyne Oscillator PCB (Het Osc 10 MHz).

3. A3A7 Sub-Synthesizer PCB (Sub-Syn 10 MHz).

4. Rear Output Reference (10 MHz).

5. 607XA-130 Oven Reference Option

2-163. The A3A2 10-MHz Reference PCB is made up of the following sections:

1. Crystal Oscillator and Phase Detector Loop

2. AC to TTL Convertor

3. Signal Control Selector Switch

4. Control Logic

5. Output Section

6. Unlock Detector

7. Optional High Stability Reference

2-164. DETAILED DESCRIPTION

2-165. Crystal Oscillator and Phase Detector

2-166. The Crystal Oscillator is a modified Colpitts type. The transistor Q2 and gates U1 are used to buffer and to convert to TTL. The transistor Q1 turns the crystal oscillator off or on. The tuning range of the mechanical capacitor C9 is enough to accomodate initial tolerances and crystal aging rates. The voltage variable capacitor CR1 provides ±100-Hz tuning range for a 2V-to-10V bias range.

2-167. Figure 2-2 is a partial schematic that illustrates the Phase Detector and Amplifier. The MOS switches in U2 are used to switch the voltage control of the crystal oscillator to a fixed bias (resistor divider R9 and R10) in the free-run mode, or to the phase detector in the phase-locked mode. In the phase-locked mode, the reference signal from the external reference input is applied to one flip-flop clock input, U5 pin 3. The signal from the crystal oscillator goes to the other flip-flop clock input, U5 pin 11. The flip-flops are connected so that the width of the pulse, which switches Q5, is the difference in time of these two signals, and the pulse witch turns on Q4 is one period of the crystal oscillator signal. The phase relationship of the stable locked condition is determined by the ratio of these pulse widths. This ratio is determined by values of the resistors R17 and R44 on the "–" and "+" inputs of operational amplifier U3. The average value of each current pulse through each resistor produces an average equal voltage across the resistors so no error voltage exists at the operational amplifier input. The operational amplifier U3 operates as an integrating amplifier with a network of R16 and C15 to produce a low frequency lead break at around 70 Hz. The operating loop bandwidth is about 300 Hz. A constant current source Q6, R18, and R19, and storage-multiplier network C18 and R18 serve to maintain constant phase detector gain and constant loop bandwidth even for inputs that are subharmonics of the crystal oscillator. The pulse rate at the phase-detector output will be the smaller of either the input frequency or 5 MHz. As an example, for a 10-MHz reference input frequency, the phase detector operation holds off every other cycle.

2-168. AC To TTL Convertor

2-169. Figure 2-3 is a partial schematic illustrating the AC to TTL Convertor. The AC to TTL Converter is made up of a standard comparator U7, associated resistors, capacitors, and diodes. The circuit drives a one-shot (U10) which is used as an external signal detector. The input capacitor C20, resistors, and diodes CR3 and Cr4 are used for level conditioning and limiting to protect the comparator. Resistors R24 throughR27 set the hysteresis to prevent spurious oscillation. The output of the converter is distributed to the signal control selector switch, phase detector, and unlock detector.

2-170. Signal Control Selector Switch

2-171. The AND/OR circuit U11, is used to select one of three inputs for the 10-MHz reference signal source. The three inputs are:

1. A3A2 PCB Crystal Oscillator.

2. 607XA-130 Oven Reference Option (Oven Reference Option Oscillator).

3. External Reference Input (AC/TTL Convertor).

2-172. The output of the signal control selector switch U11 goes to the output section. The control is a one-of-three selection and comes from the logic section. The High Stability Ovened Oscillator signal (Option -130 is also controlled by the gates of U13 to provide additional isolation between this signal and the external reference input signal.

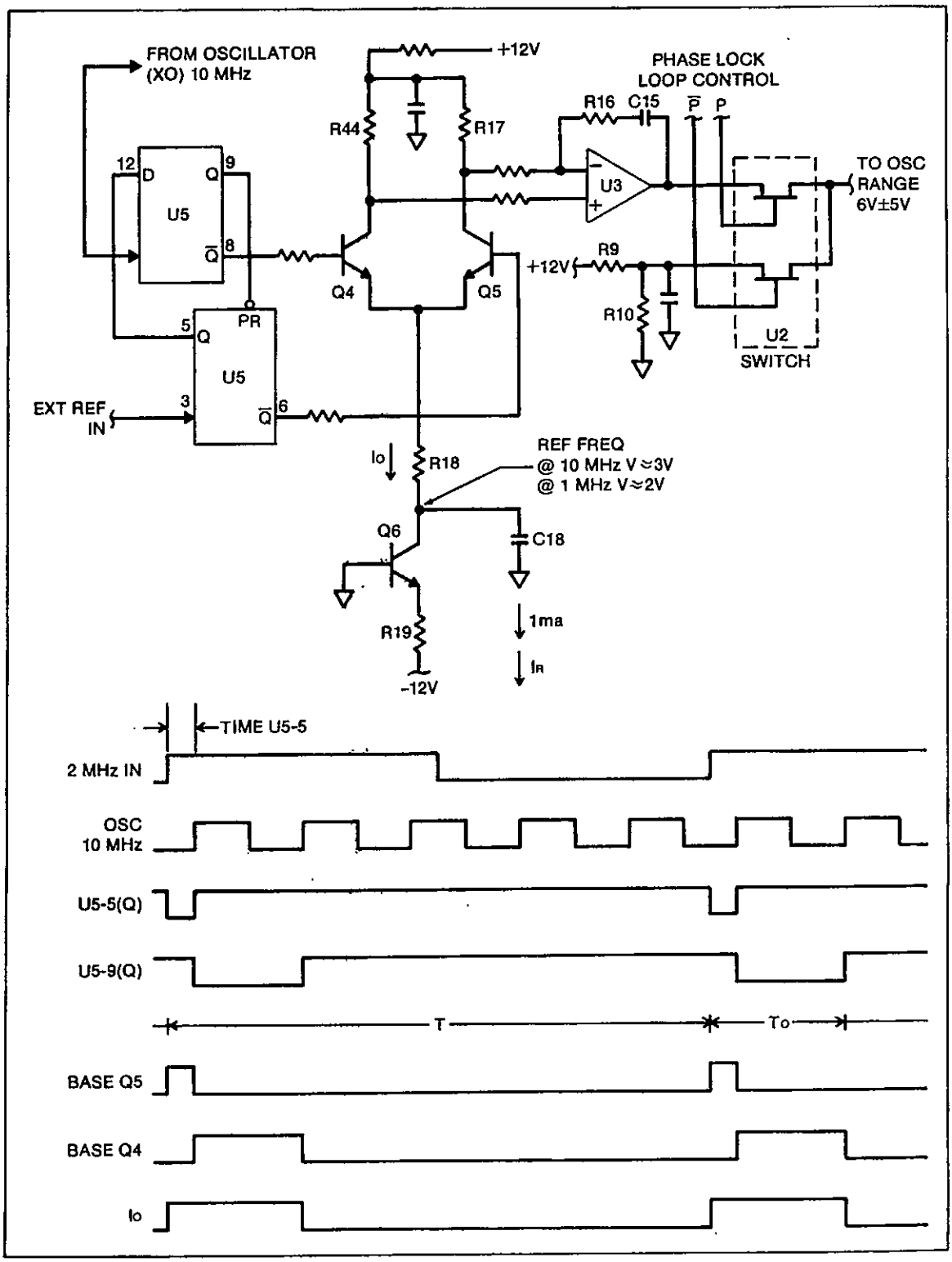

Figure 2-2. Phase Detector and Amplifier

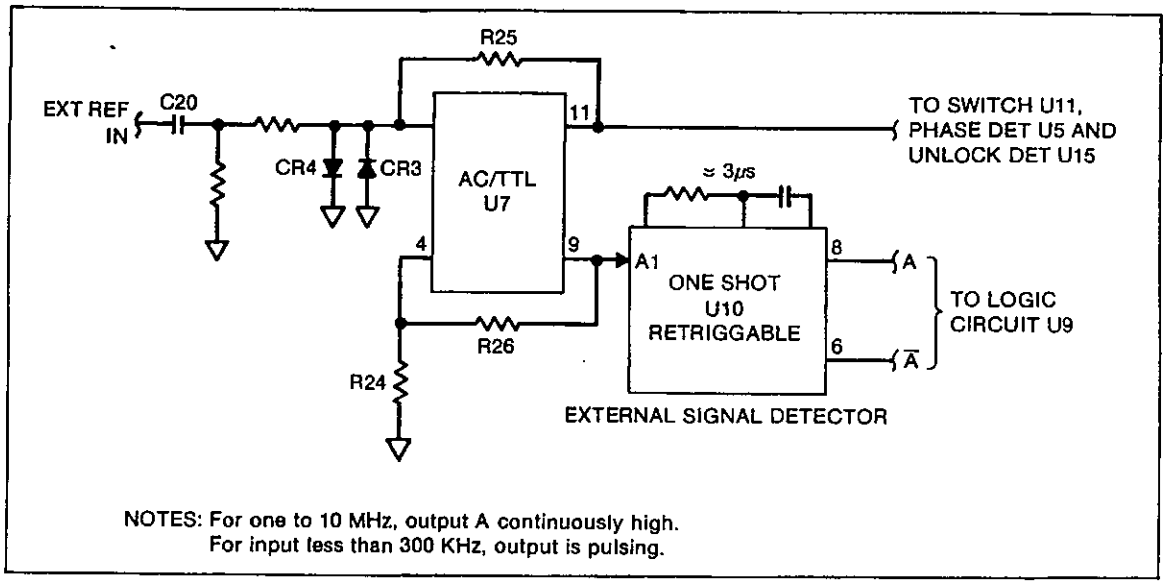

Figure 2-3. AC/TTL Converter

2-173. Control Logic

2-174. The Control Logic Section consists of gates, buffers, and a one-shot (U4, U6, U9, U10, and U13). The three inputs to the logic section are:

1. "A", U10-pins 8 and 6 which is the external signal detector output. The signal detector U10 is a retriggerable one-shot with a pulse width of three microseconds, which makes output u10-8(A) continuously high for signals greater than 1 MHz.

2. EXTLK H (P1 pin 6) which is exercised by the Controller. The signal is set high when the external input is to be phase-locked (shift 60) and set low when the external input is to be wideband (shift 61).

3. STDXO H (P1 pin 7) which is set by switch S1 to a low when the 607XA-130 Oven Reference Option is installed. Since the connector pins go through the plate, S1 can be overridden from either side of the plate. The switch can be used to manually select the crystal oscillator or the Oven Reference Option Oscillator as a signal source.

2-175. This control logic section is combinational logic that produces four outputs:

1. "EXT," U6 pin 4, which controls the external reference (EXT) to the signal control selector switch U11 pin 3.

2. "HS," U6 pin 6, which controls the high stability (HS) input to the signal control selector switch and to gates U13 to control the HS enable line to J8.

3. "XO," U6 pin 10, which controls the XO input of the switch andon/off operation of the PCB crystal Oscillator (XO) through U4 pin 6.

4. "P," U4 pins 2 and 4, which controls the switch U2 in the phase-,ocked loop path (P).

2-176. The control logic relationships are listed in Table 2-7.

2-177. Output Section

2-178. The output section consisting of gates and buffers U8 and U12, has the following four outputs:

1. The PD 10 MHz output connector (A3A2P1) goes to the main loop Phase Detector on the A3A1 Phase Detector PCB. The signal is double buffered in the AND gates (U8-3, U8-6) to provide isolation when the signal is turned off. This 10-MHz signal is controlled with the line FIX 10H (P1 pin 5) determined by the Controller.

2. The Het 10-MHz signal at J5 is double buffered by U8-11 and U8-8 to provide isolation when the signal is programmed off. This signal is controlled from the A4A8 Heterodyne Oscillator PCB on connector J5 and is multiplexed on the signal path along with the AC-coupled ECL level signal. The TTL signal is converted to ECL by resistors, R29, R30, R31, and AC-coupled through capacitor C24. The DC control level is separated from the ECL signal by a low-pass filter (L8, C23) and is applied to the control inputs of U8 pin 9 and U8 pin 13. A low inhibits the ECL signal.

Table 2-7. Control Logic Truth Table

	SIGNAL	STATE
INPUTS	EXT. INPUT SIGNAL	N Y N Y N Y N Y
	WIDEBAND (NOT EXT LKH)*	N N Y Y N N Y Y
	HS OPTION (NOT STDXO H)*	N N N N Y Y Y Y
OUTPUTS	EXT (U6-4)	N N N Y N N N Y
	HS (U6-6)	N N N N Y N Y N
	XO (U6-10)	Y Y Y N N Y N N
	P (U4-2, -4)	N Y N N N Y N N

3. The SS 10-MHz output connector to the A3A7 Sub-synthesizer PCB is P1 (A3A7J1). The Output signal is buffered by U12-4 and U12-6 in parallel.

4. The 10-MHz REF signal output to the rear panel Connector J7 is also buffered by U12-10 and U12-12 in parallel.

2-179. Unlock Detector

2-180. The Unlock Detector is made up of flip-flop U15 and a one-shot U14. The Unlock Detector provides a status output which indicates that the crystal oscillator is not locked to an applied input reference signal. The flip-flop input (U15 pin 3) is clocked by the external reference output from the AC TTL circuit, and the signal at the D (U15 pin 2) input comes from the crystal oscillator. As long as the two signals are not shifting in phase, the output of the flip-flop will not change. However, if the phase between the two signals is changing, then the output of the flip-flop will be changing at a rate equal to the frequency difference between the two signals, which is in general greater than 100 Hz (the pull range of the crystal oscillator). This output, applied to the one-shot U14, triggers the one-shot on a positive transition. The one-shot is retriggerable and has an output pulse width of about 0.2 seconds. So, it operates as a pulse stretcher providing the microprocessor status information available as RNULK L at connector P1 pin 4. Thus, a negative output on this line indicates that the crystal oscillator (6070A/6071A system reference) is not locked to a externally applied reference and that the two frequencies are not within atolerance range of each other, or that some other fault exists. R45 and C30, (the crystal oscillator input to the flip-flop U15 pin 2) shifts the transition point in this signal away from the clock transition point to avoid false indications on the status line.

2-181. A3A3 Delay Discriminator PCB Circuit Analysis

2-182. Refer to the System Block diagram and the A3A3 Delay Discriminator PCB located in the 6070A/6071A Schematic Manual.

2-183. The A3A3 Delay Discriminator PCB, in conjunction with the Delay Cable Assembly, provides phase noise suppression of the 250-MHz to 520-MHz signal supplied by the A3A5 VCO PCB. The delay discriminator circuit is tuned to the selected A3A5 VCO operating frequency by logic signals from the microprocessor. Phase noise suppression of approximately 20 dB is achieved by the delay discriminator. The A3A3 Delay Discriminator also incorporates FM modulation circuits including a range attenuator and mode selection which disables the delay discriminator circuit and allows the A3A5 VCO to be directly frequency modulated, thus providing greater FM deviation capability.

2-184. The VCO signal enters the A3A3 Delay Discriminator PCB via A3A5J1 at a level of +6dBm and an impedance of 50 ohms. This signal is amplified 10 dB by U1 and split into two separate signals at the output of U1 by hybrid W1. One signal is attenuated 4 dB by R10, R11, and R12 and is routed to A4A4 Modulator/Divider (A4A4J13). This signal becomes the main output of the Synthesizer Section. The other signal is amplitude-limited by CR1 and CR2, amplified 10 dB by U2, and attenuated by CR3 and CR4. This attenuator is electrically adjustable via U5 and is part of a leveling loop including (T1, T2, T3, CR14, U5, and CR3 and CR4). This loop holds the signal from U6 pin 1 constant in amplitude at CR4. The amplitude-controlled signal is then low-pass filtered (via L15, L16, L17, and C15 through C20) and is amplified 10 dB by U3 and 6 dB by U23 to a level of approximately +22 dBm at U23 pin 3.

2-185. The high power signal from U23 pin 3 is applied via E7 to quadrature coupler W2 which splits the power between terminals E8 and E9. The signal at E9 is phase shifted -90 degrees compared to the signal at E8 (0-degree phase). The PI signal can be either a high or low logic signal and is applied to the A3A3 PCB at P1 pin 2. Diodes CR24 through CR27 act as a reversing switch controlled by the PI logic signal to cause the 90 degree shifted signal to appear at the DELAY OUT jack (A3A3J11) and the 0-degree phase signal to appear at C21 or the 0-degree signal

the appear at A3A3J11 and the 90 degrees signal to appear at C21, depending on the logic state of PI. The net effect of this action is to cause the relative phase between C21 and A3A3J11 to switch 180 degrees in response to a change in the logic level of PI. The level at A3A3J11 and C21 is approximately +18 dBm.

2-186. Quadrature coupler W3 acts in a similar manner to W2, causing the signal at E12 to be split between E13 and E14. The signal is phase shifted -90 degrees at E14 compared to the zero degree phase shift at E13. Diodes CR18 through CR21 act to select either the 90 degree signal or 0-degree signal in response to a logic level from PI2. This signal is greater than +11 dBm and is applied to phase detector U6 pin 4.

2-187. The signal at A3A3J11 passes through the A7 Delay Cable Line. The delay cable delays the signal 230 nsec and attenuates the signal 6 dB to 9 dB, depending on frequency, and returns the signal to the A3A3 Discriminator PCB via A3A3J12.

2-188. Diodes CR6 through CR11 and inductors L9 through L14 form a three-section tunable bandpass filter which acts as a ±180-degree electrically tunable phase shifter when operating near the center of its pass band. The phase-shifted output passes through transformers T1 and T2 which act as a directional coupler to tap off 10 percent of the power. This power is applied to the leveling loop via detector CR14 and CR15, which maintains the level of phase detector U6 pin 1 constant at +5 dBm. Potentiometer R24 sets this level. Potentiometers R48 and R50 adjust the shape factor of the tunable bandpass filter to best optimize the response over the frequency range.

2-189. The phase shifter (tunable bandpass filter) is incorporated in a feedback loop designed to hold the output of phase detector U6 to precisely 90 degrees (zero volts out). This loop functions as follows. The voltage from U6 pin 2 (zero volts) is routed to voltage comparator U14 pin 3, and the error voltage is amplified by U12. Potentiometer R86 is used to trim the offset voltage which sets the voltage out of U6 pin 2 (TP5) to precisely zero volts. The error voltage from U12 is applied to operational amplifier U4 which amplifies the error voltage to cause the electrically tuned phase shifter to be adjusted in phase until the output of U6 pin 2 returns to 90 degrees (zero volts out). The Phase Shifter DAC voltage (PHV) is a tracking voltage which adjusts the tuning voltage to the bandpass filter/phase shifter via U4 to keep the filter operating in the center of its bandpass regardless of operating frequency. The PH voltage is generated from data stored in the calibration EPROM (A2A1U11) via a DAC located on the A3A8 Synthesizer Control Buffer PCB. Potentiometer R45 adjusts the PH voltage. Operational amplifier U10 and diodes CR22 and CR23 form a symmetrical clamp that prevents the error voltage from exceeding a level that might cause the phase shifter to be adjusted out of its bandpass range. The clamp voltage is adjusted as a function of frequency by applying the PH voltage to U10 which controls the diode conduction point.

2-190. The circuits described act together to form a delay discriminator that tracks the incoming VCO frequency. The output of the discriminator at TP5 is amplified by a descrete operational amplifier having very low noise (Q6, Q1, Q2, and Q3). The signal is applied to J1 pin 6 (output to VCO) via switches/attenuators Q4 and Q9. This feedback loop causes the noise of the VCO to be improved by approximately 20 dB.

2-191. In order to eliminate potential hangup modes, an acquisition/lock-on circuit is incorporated. The zero voltage signal from the delay discriminator output (U6-2) is amplified by U14 and compared to a reference voltage set by R81 and R82 to insure that anytime this voltage exceeds ±1 volt the comparator U16 will fire U13 (an 8-msec one-shot).

2-192. Firing one-shot U13 causes Q4 to open and Q9 to close, disconnecting the delay discriminator from the circuit. Firing the one-shot U13 also turns on Q5, which establishes the correct lead-lag network for the main phase lockloop operating with the discriminator loop disconnected.

2-193. Potentiometer R146 adjusts the relative voltage to Q4 and Q5 so that the transition between the two modes is smooth and controlled. When one-shot U13 fires, the edge of the pulse is differentiated by C87 and C88 causing the clamp (U10, CR22, and CR23) to close momentarily. This closure puts the phase shifter momentarily in the center of its tuning range, thereby establishing a standard starting point for the acquisition of the discriminator loop. The acquisition process is initiated by a change in the PI or PI2 signals which are sensed by the comparators (U16-1 and U16-2). Acquisition is complete when the 8-msec time-out is completed and the output of U6 is within the acceptable band (around zero volts).

2-194. The turn-on self-check routine monitors DDINV while the frequency is changed to verify that it pulsed during the acquisition cycle and then remains low. If DDINV continues to pulse, this is an indication of a fault and is annunciated as self-test error code 040 in the AMPLITUDE display or as a frequency UNCAL error code of 020.

2-195. Switches U18, K2, and K3 are used in conjunction with scaling resistors U17 to attenuated the audio modulation signal DIFM coming from the phase detector A3A1P2. Logic signals DIRN(0-2)H and DIMOD(H) control the attenuator ranges via drive U20.

The output of the range attenuator is applied to the negative input of the discrete operational amplifier (Q6, Q1, Q2, Q3) causing the delay line descriminator stablized oscillator to be FM modulated by the audio modulation signal. A small portion of the range attenuated audio modulation signal is further attenuated by R67 or R53 and applied to the negative terminal of U14. This signal is used to eliminate modulation signals in the phase zeroing loop (U14, U12, and U4).

2-196. Relay K1 sets the instrument in the high deviation mode via the VCO(H) logic signal which is used to disable the delay discriminator by removing 12 volts from the RF amplifiers U2 and U3 via switch Q10 and Q11. In this mode, the FM modulation audio signal is applied directly to the VCO modulation terminal via the same audio range switch U18, decoder U21 and U20, and relays K3 and K2. Relay K4 disconnects R93 reducing the noise gain of the operational amplifier (Q6, Q1, Q2, and Q3). In the high deviation mode, the amplifier gain is adjusted to provide 10 times greater modulation for each range step than is provided in the normal mode. Potentiometer R103 adjusts the FM deviation level in the high FM deviation mode at 10 kHz rate. Potentiometer R110 adjusts the high deviation mode main loop bandwidth to 2 kHz.

2-197. The function of Q7 is to increase operational amplifier (Q6, Q1, Q2, and Q3) loop gain at frequencies greater than 380 MHz when in the normal mode, offsetting a decrease in VCO modulation sensitivity.

2-198. A3A4 N/1 Divider PCB Circuit Analysis

2-199. BRIEF DESCRIPTION

2-200. Refer to the System Block Diagram and the A3A4 N/1 Divider Schematic located in the 6070A/6071A Schematic Manual.

2-201. The programmable A3A4 N/1 Divider PCB is part of the main (250 MHz to 520 MHz) synthesizer loop and provides control of the 0.1, 1, 10, and 100 MHz digits. The divider input is the output of the A3A6 SSB Mixer and the output, which scales the input of the programmed division to 2 MHz, goes to the A3A1 Phase Detector, N/1 input. The reference frequency for the A3A1 Phase Detector is 2 MHz.

2-202. The N/1 Divider has two major sections (refer to Figure 2-4):

1. Divider
   a. Dual Modulus, 10/11 Prescalar
   b. Counter
   c. Rate Multiplier
2. Digital
   a. Latches (Two Levels)
   b. Load Circuit

2-203. The Divider uses the dual modulus prescaler with a two section counter and the rate multiplier to divide the input to 2 MHz in a ratio with a fractional increment of 0.05. The ratio ranges from 124.85 to 259.85 in the normal operating range of 250 MHz to 520 MHz in 100 kHz steps. The offset in the divider ratio relates to the SSB Mixer offset. The divider counting cycle is controlled by the counter logic.

2-204. The programmed division is set by the latches. The latches accept signal input from the controller and program the counters in parallel on command from the load circuit. The Load Circuit is under control of the microprocessor controller and is synchronized to the divider output.

2-205. DETAILED CIRCUIT ANALYSIS

2-206. Divider

2-207. The 250 MHz to 520 MHz signal is divided down in 2 MHz in 100 kHz steps by programming a ratio of 124.85 to 259.85 in 0.05 fractional increments. The main components of the divider are: dual modulus 10/11 prescalar U13, two counter sections (U14, U15, and U16), a rate multiplier fractional counter (U4, U5, U7, and U8), and counter logic (U17).

2-208. The fast (600 MHz) dual modulus prescaler U13 is used in conjunction with slow (100 MHz) programmable counters to produce a fast-programmable (570 MHz) divider.

2-209. The input signal to the dual modulus prescaler U13 is conditioned to a proper level by limiting diodes CR1 and CR2 and associated resistors R1 through R6. The prescaler U13 simply scales the input signal by a ratio of 10 or 11 depending on the mode control line. A high on U13 pin 13 forces aprescaler ratio of 10. A low on U13 pin 13 forces a prescaler ratio of 11. There are two types of outputs: an ECL output and a TTL output. The ECL output is fed to the counters and the counter logic, and the TTL output is fed to a TTL D-type flip-flop U20.

2-210. The dual modulus prescaler U13 is imbedded in a two counter system which has a units counter U14 and a tens and hundreds counter, U15 and U16 (also called "A" and "N" counters). The "A" counter counts only the prescaler cycles of count by 11. Therefore, the total count, N(c), of the counter part of the divider is:

$$N(c) = (N-A)*10 + A*11$$
$$= N*10 + A*1$$

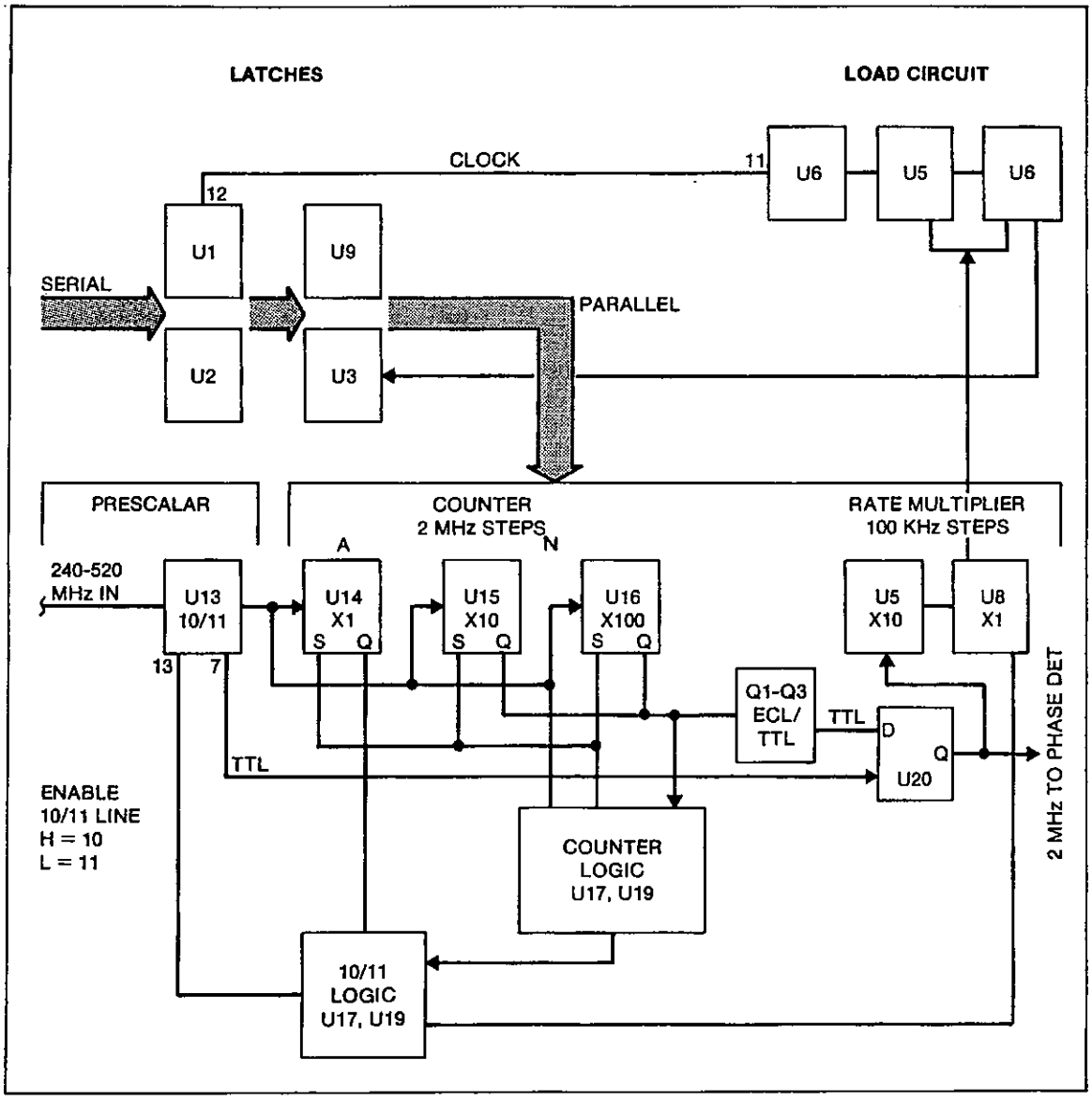

Figure 2-4. A3A4 N/1 Divider PCB Block Diagram

2-211. The counter logic determines when the counters halt and when they load the programmed number. The dual flip-flop U17 and gates in U19 are used to anticipate (early detect) the end count and load the programmed number at the proper time to the counters U14, U15, and U16, through the "S" lines (count up, down/load/hold) and "CE" (enable) lines. Flip-flop U17 and AND gate U19-2 are used as well to logically sum the inputs (from U14 "A" counter and the Rate Multiplier) to the 10/11 mode line for an "11" count of prescaler U13. Flip-flop U17 is necessary to accommodate race conditions, ambiguous states, and delay of the outputs from the counters. It is clocked by the prescaler U13 output and synchronized to counters.

2-212. The ECL/TTL converter (which consists of U19, transistors Q1, Q2, and Q3, diode CR3, associated resistors, and one clocked D-type flip-flop U20) is used to generate a TTL output that is not ambiguous. The TTL output from the dual-modulus prescaler U13 clocks the information from the counters U14, U15, and U16 on the "D" input U20-2. The "Q" output U20-5 becomes the output of the N/1 Divider PCB at connector J13 and is also present at test point TP5.

2-213. Figure 2-5 is a partial schematic of the rate multiplier. The rate multiplier produces the fractional part of the division. The rate multiplier is made up of a flip-flop U5, some gates of U4, inverter U7, and a decade rate multiplier, U8. This combination produces a single bit tens decade and a BCD units decade, U8, for the fractional part. The rate multiplier follows the ECL/TTL converter and produces a pulse train which has a programmed number N(r) of pulses for a frame of 20 cycles of the output of the PCB. The programmed number ranges between 0 and 19. The rate multiplier output, available at test point TP2, is translated to ECL level by resistors, R11, R12, and R13, and combined in the mode line of the prescaler through gates of U19. Thus, the prescaler counts by 11 for every rate multiplier output pulse and the fractional part, N(f), of the overall division ratio becomes N(f) = N(r)/20.

2-214. Notice that the pulses are not necessarily equally spaced in time. This produces jitter on the N/1 Divider output at a possible lowest rate of 100 kHz. This spurious product is filtered out by the transfer characteristics of main loop response and the phase detector low-pass filter.

2-215. The total division ratio is found by combining the counter division, N(c), and rate multiplier division, N(f). This total division ratio becomes:

$$N(\text{total}) = N(c) + N(f) = 10\,N + A\,N(r)/20.$$

2-216. The frequency (fin) of the input for 2 MHz output is:

$$fin = 20N + 2A + N(r)/10 \text{ MHz}$$

2-217. The numbers programmed to the divider are not the division ratio; they do not correspond directly to the front panel display either. The schematic shows these numbers, N, A, N(r), with respect to programmed frequencies in the fundamental band, a 2 MHz (reference) frequency, and the offset frequency introduced in the SSB Mixer. The program number for the divider can be found by:

1. Referring the output frequency to the fundamental band (250 MHz to 520 MHz).

2. Subtracting the 201 kHz offset introduced in the SSB Mixer.

3. Partitioning the number into two parts between the 10-kHz and 100-kHz digit. Lower order digits are for the Sub-Synthesizer.

4. Using the 100-(BCD) kHz and 1-MHz (single bit only) digits directly.

5. Scaling the remaining 2-MHz and greater digits to a 2-MHz reference, by dividing by 2.

2-218. The program number, as shown on the schematic, consists of three BCD digits times 2 MHz reference (X1, X10, and X100 BCD) digits, a single bit digit times 1 MHz (X1, or 100 kHz X10 single bit), and a one BCD digit times 100 kHz (X1 BCD). The counter and the rate-multiplier receive this input programmed number from the latches.

2-219. Digital Latches and Load Circuit

2-220. The latches, (U1, U2, U3, and U9) which control the divider are arranged into two levels (ranks). The first level U1, and U2, is loaded directly by the Controller via the serial interface bus. The serial data DNTAH is distributed into the latches by the address, NAB(0-2)H, and select, NSEL(0-2) > lines (P1 pins 1-7). The most significant bit of the first level latch is used for initiating the action of the load circuit to transfer of the information from the first level latches to the second level latches in parallel into the counter and rate multiplier program inputs.

2-221. The load circuit is intiated by a positive transition of this bit (from U1-12) as determined by the controller (refer to Figure 2-6). (This bit is also inverted by U10-13 to the connector, P1 pin 8, as a test bit, N1TST H.) The load circuit is further synchronized with the divider output with the frame rate of the rate multiplier. The trailing edge of the 10-microsecond, negative-going pulse from the load circuit clocks the new frequency data into the second level latches. A positive version, available at TP1, is sent to the PCB output connector, P1 pin 14, (as TMCNT H) and is used to update the Sub-Synthesizer frequency on the leading edge.

2-222. The two level latches (serial to parallel), the 10-microseconds delay time in the signal (TMCNT H), (a match to synthesis path delay), and the synchronization of the edges simultaneously update the frequency control to the dividers in both the main loop and the sub-synthesizer loop to minimize phase discontinuities in the generator output during frequency switching.

2-223. To prevent a hangup if the divider is programmed to zero, U10 is connected between the latches and counter program input in the most significant digit. If a zero is present on the inputs of U10, the output will be a one. (Both one and two input values are valid.)

2-224. A3A5, A3A10 VCO Resonator PCB Circuit Analysis

2-225. Refer to the System Block Diagram and the A3A5, A3A10 VCO Resonator PCB Schematic in the 6070A/6071A Schematic Manual. The A3A5 VCO Resonator VCO PCB and the A3A10 VCO Resonator PCB are identical; consequently, the same schematic applies to both PCBs. The A3A5 PCB is located on top of the Synthesizer Module, and the A3A10 is located on the bottom of the Synthesizer Module.

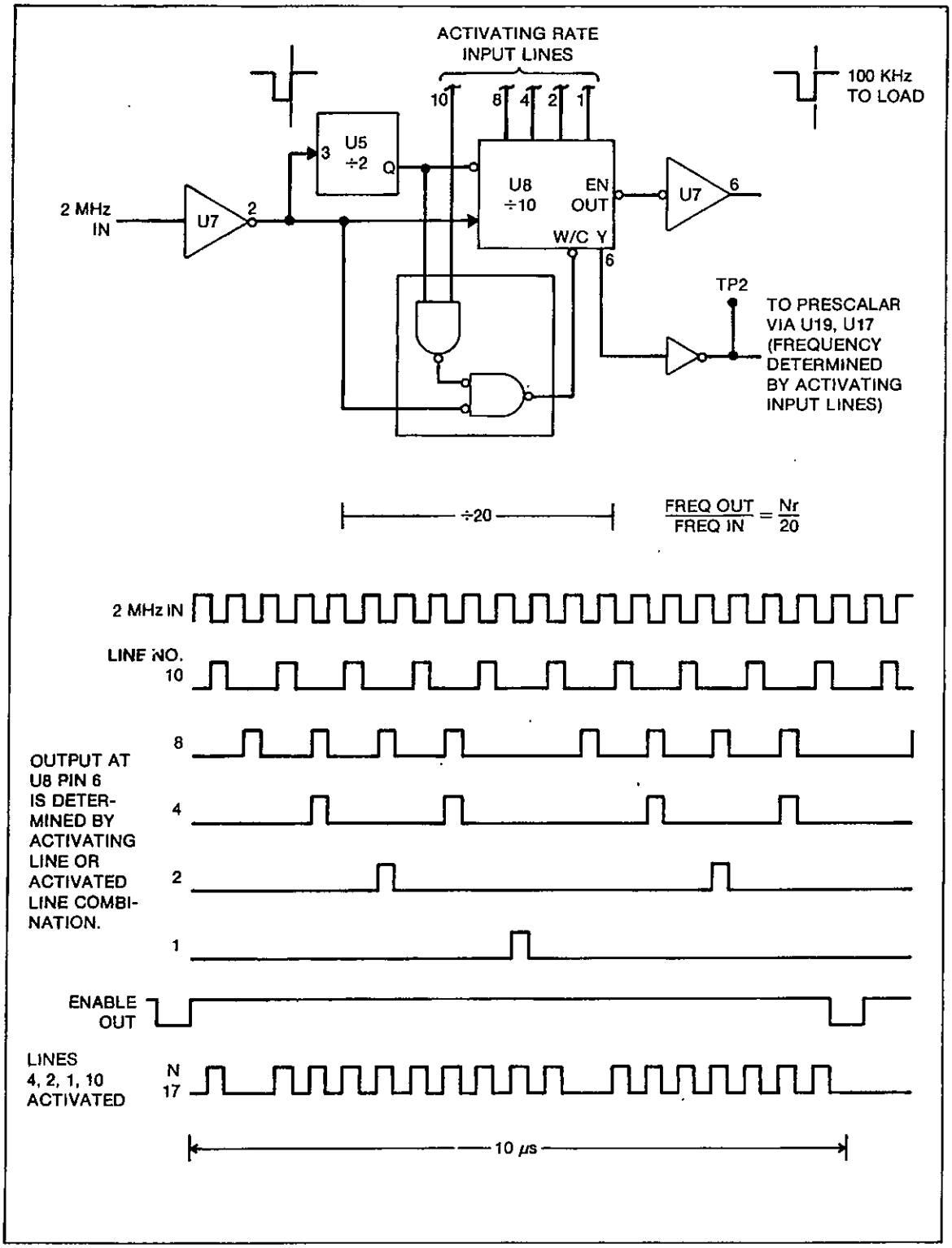

Figure 2-5. Partial Schematic of Rate Multiplier

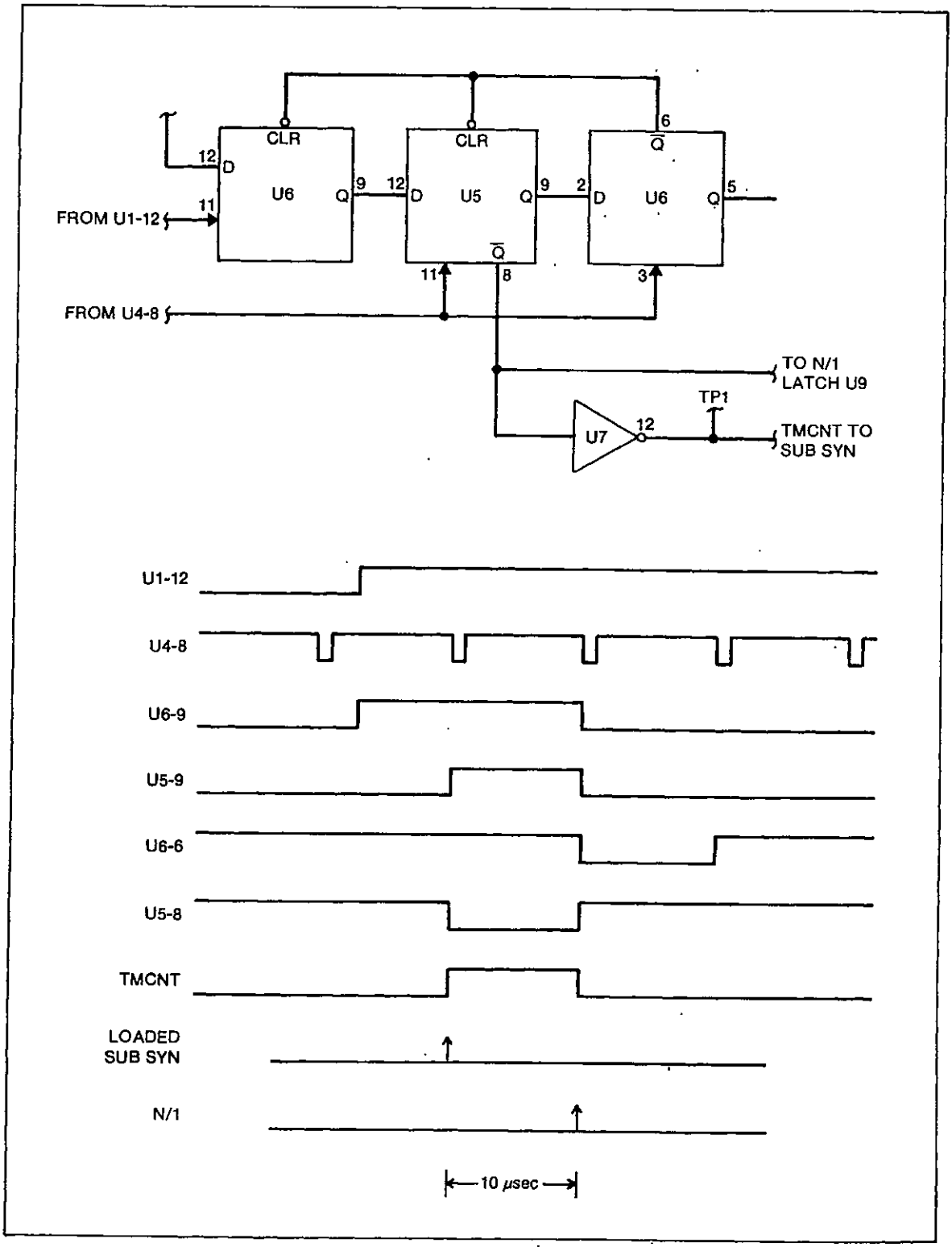

Figure 2-6. Frequency Load Cycle

2-226. Each VCO Resonator PCB is a relatively low noise, voltage-controlled oscillator capable of being electrically tuned over a minimum frequency range of 250 MHz to 520 MHz. The A3A5 PCB and the A3A10 PCB make up a matched pair (frequency tracking) of VCOs. The A3A5 VCO Resonator PCB is used as the main loop VCO, and the A3A20 Resonator VCO PCB is used as the cleanup loop VCO. The following circuit analysis applies to both PCBs.

2-227. The oscillator consists of a transistor which is physically located on U1 and a resonator (CR1, CR2, and L5 through L8). Inductors L5 through L8 are sections of stripline transmission line. Diodes CR1 and CR2 are voltage-controlled variable capacitance diodes. The main frequency control voltage for phase-locking is applied to the cathodes of CR1 and CR2 through E1, whereas the wideband FM modulation signal is applied to the anodes of CR1 and CR2 through E5. The tuning coefficient varies with frequency and is roughly 20 MHz per volt at 250 MHz increasing to about 30 MHz per volt at around 320 MHz, and then decreasing to about 10 MHz per volt at 520 MHz.

2-228. The buffer U2 consists of several amplifier sections used to isolate the two output paths from each other and from the oscillator circuit. This minimizes pulling of the oscillator by external circuit effects and prevents signals present at one output port from affecting the other output port.

2-229. A3A6 Single Sideband Mixer (SSB Mixer) PCB Circuit Analysis

2-230. Refer to the System Block Diagram and the A3A6 Single Sideband Mixer PCB Schematic located in the 6070A/6071A Schematic Manual.

2-231. The A3A6 Single Sideband Mixer (SSB Mixer) operates in the main synthesizer loop in conjunction with the programmable A3A4 N/1 Divider, the A3A1 Phase Detector, and the A3A10 VCO to synthesize the fundamental frequency range from 250 MHz to 520 MHz. The SSB Mixer adds in a 200-kHz to 300-kHz signal from the sub-synthesizer to provide lower order (1 Hz to 10 kHz) digits of resolution.

2-232. The SSB circuits consists of a lower sideband mixer followed by a phase-locked loop (PLL) functioning as a tracking filter (also referred to as a clean-up loop). The lower sideband mixer uses quadrature mixing techniques. The tracking filter employs a VCO, a Frequency-Phase detector, frequency scalers (dividers), loop amplifiers, and control circuits.

2-233. The tracking filter reduces the unwanted signals in the output of the LSB mixer to prevent intermodulation spurious generation in the main loop. The tracking PLL bandwidth is controlled because of its influence on the main loop angle modulation characteristics.

2-234. SSB MIXER THEORY

2-235. The single sideband mixer consists of two phase shifters and two mixers. The low frequency in the 200-kHz to 300-kHz range is subtracted from the high frequency in the 250-MHz to 520-MHz range. Figure 2-7 is a simplified schematic of the A3A6 Single Sideband Mixer.

2-236. The low frequency is generated and split into two signals in a 90-degree phase relationship in U16 and associated low-pass filters. The input signal frequency at J1 is actually four times the mixer input signal frequency. This input signal frequency is in the 800 kHz to 1200 kHz range and drives a divide by four U16 which is connected as a two-bit ring counter and produces two square waves in quadrature (90 degree phase relationship). This is illustrated in Figure 2-8. The one signal from U16 pin 5 is fed through low-pass filter (C41, L19, C43, C42, L10, C44, and L11). The resistors, R60, R61, R62, and R63 scale the signal to the proper input level (about -2 dBm) for the mixer U12. This signal is at a relative 0 degrees. The other output of U16 from pin 8 goes through the low-pass filter (C45, L12, C47, C46, L13, C48, and L14) and is scaled by resistors R64, R65, R66, and R67 to a proper level for mixer U11. This signal is at a relative phase angle, -90 degrees.

2-237. The high frequency inputs to the mixers are generated from the input at J2. The frequency is buffered by amplifier U7 and attenuated by the resistor pad, R71, R70, and R72, to provide reverse isolation for the input at J2. Amplifier U13 provides some limiting and power gain to drive the 3 dB quadrature hybrid W1. This device produces a 90-degree phase shift between two equal amplitude signals. The one output of W1 drives the LO port of mixer U12 at +7 dBm level at 0 degrees relative phase, and the other output of W1 drives the LO port of mixer U11 and +7 dBm at -90 degrees relative phase. The isolated port of W1 is terminated in a resistor R59.

2-238. Because of the phase relationship of the outputs of the two double-sideband, suppressed-carrier mixers, the summing of the two composite signals (in resistor network, R68 and R69) results in the upper sideband component being suppressed. Therefore, the only large signal is the lower sideband signal which is larger than the others by about 25 dB. This signal is amplified by U6 to drive the divider U5.

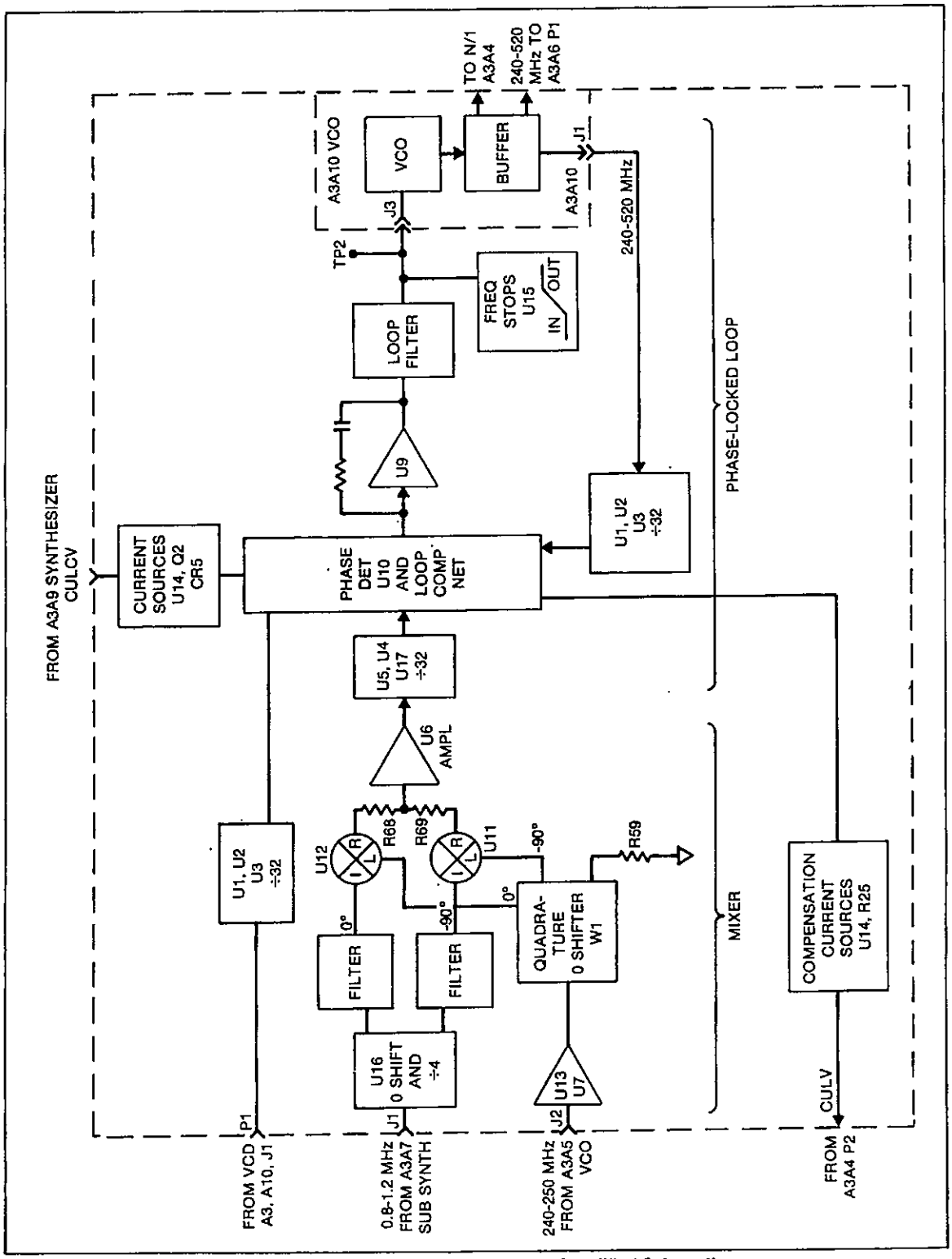

Figure 2-7. A3A6 Single Sideband Mixer, Simplified Schematic

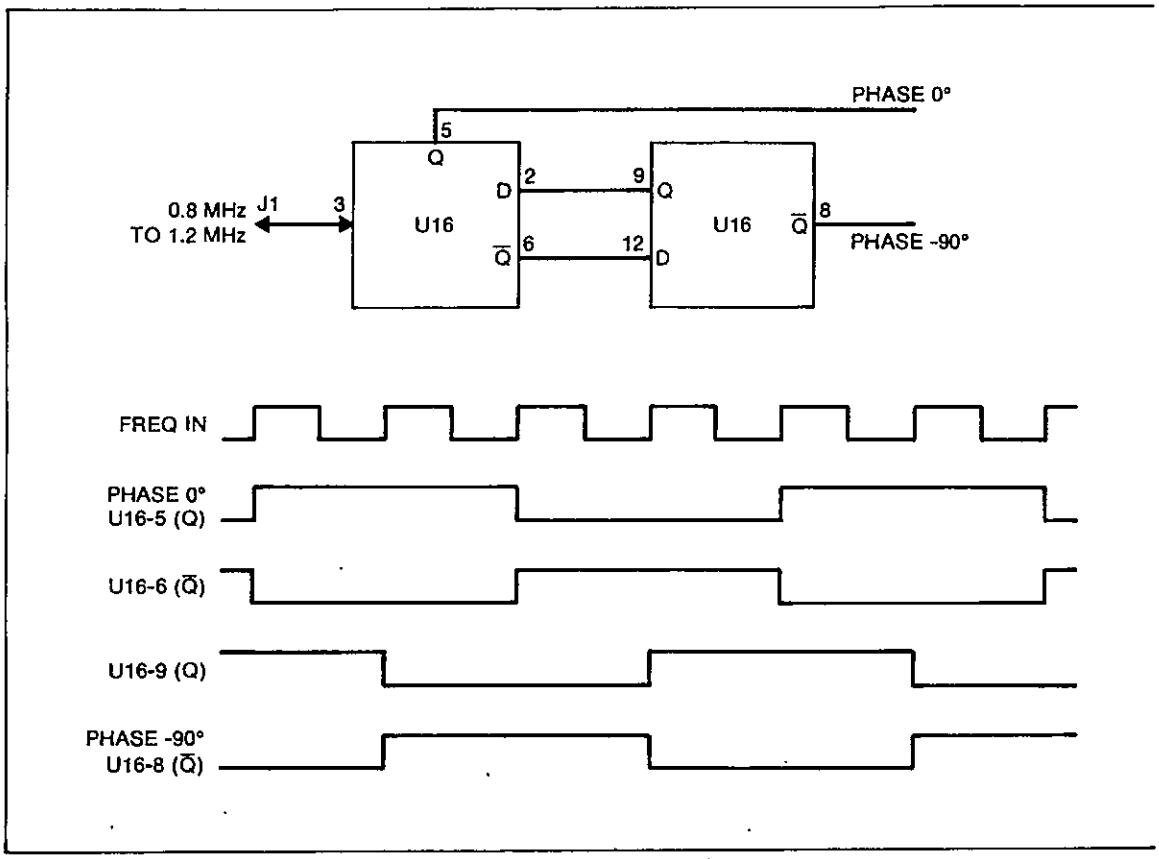

Figure 2-8. Low Frequency Phase Shift, U16

2-239. PHASE-LOCKED LOOP (CLEANUP LOOP)

2-240. The cleanup loop, a phase-locked loop (PLL) tracking filter, follows the mixer circuits and performs a cleanup function by reducing the unwanted signals and by suppressing the generation of spurious signals in the main loop divider. The cleanup loop consists of a voltage controlled oscillator (VCO), frequency scalers, a frequency/phase detector (with the loop compensation network), a loop amplifier, a loop filter, and frequency stops for the VCO.

2-241. The frequency/voltage characteristics of the VCO (A3A10) matches that of the main loop VCO (A3A5). This is necessary since common information for loop gain compensation is used for both loops.

2-242. Two divide-by-32 frequency scalers are used in the cleanup loop. The SSB Mixer drives one scaler (divider chain). This divider chain has a divide-by-four prescaler U5 followed by a dual flip-flop U4 connected as a divide-by-four and followed by one flip-flop (1/2 of U17) connected as a divide-by-two. The VCO drives the other divider chain consisting of U1, U2,and U3.

2-243. The two divider chains drive the frequency/phase detector which consists of detector U10, switching diodes, CR1 through CR4, and the switched current sources embodied in U14. Figure 2-9 is a simplified schematic of this frequency/phase detector circuit. The mixer divider drives the R (reference) input of the frequency/phase detector and the VCO divider drives the V (variable) input of the frequency/phase detector. If the V input is low in frequency or lagging in phase, the U (up) output acts with diodes CR3 and CR4 to cause the negative current source to slew up the voltage output of the integrating operational amplifier U9. This (through the loop filter network) forces the VCO up in frequency. (The VCO has a positive frequency-voltage transfer.) Similarly, if the V input is high or leading, the D (down) output works in conjunction with diodes CR1 and CR2 to cause the positive current source to steer the VCO down in frequency. The loop dynamics allow the circuit to settle to a steady state, in which the D output pulse width is just wide enough to account for the offset current through resistor R53.

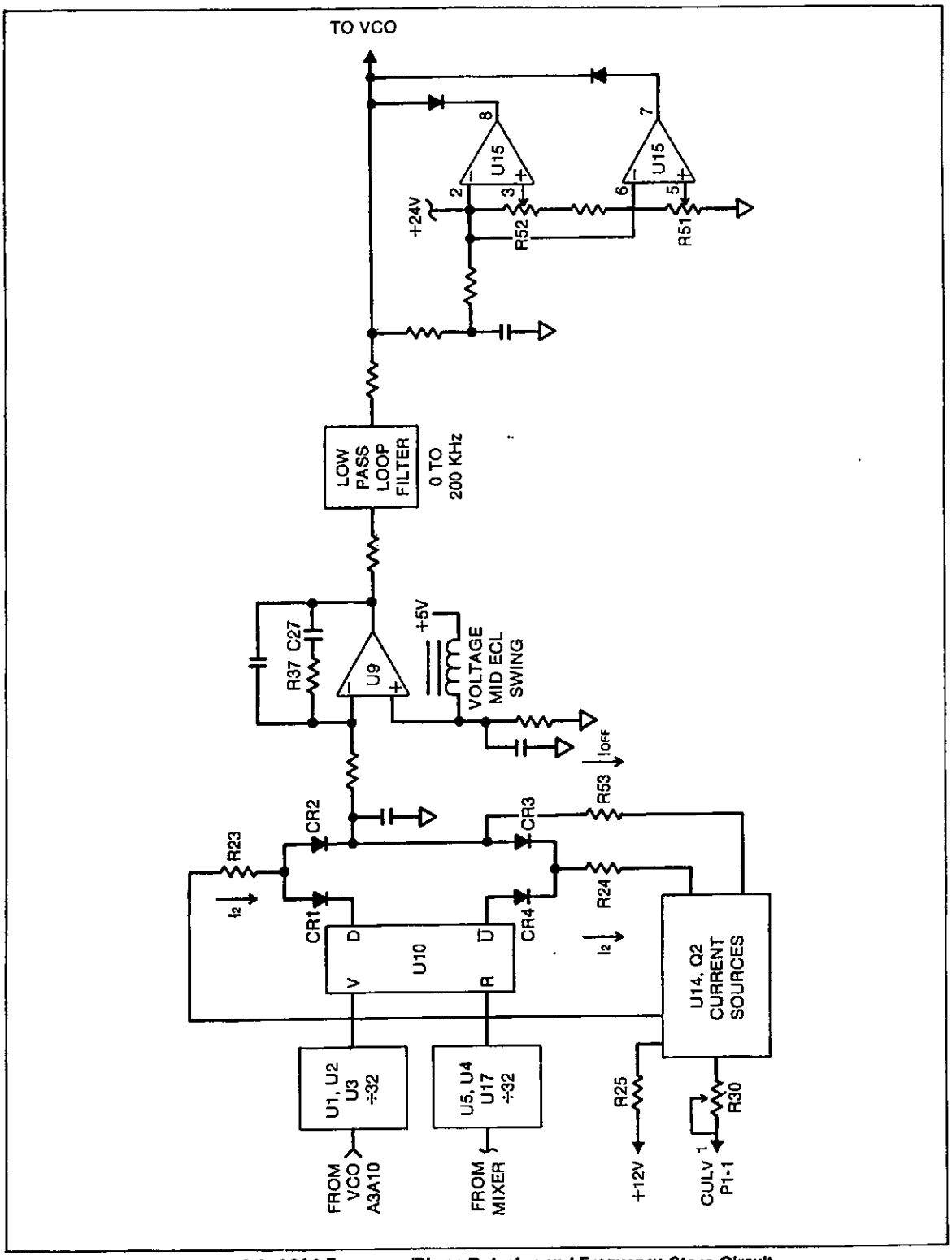

Figure 2-9. A3A6 Frequency/Phase Detector and Frequency Stops Circuit

2-244. The current sources (U14, Q2, CR5, and associated resistors) are designed so that the up current and the down current are equal and the offset current is about one-fourth of this value. The transistor Q2 is used for beta multiplication. The steady state phase detector pulse is therefore about 25 percent duty cycle. The offset avoids the crossover distortion which exists at zero pulse width in the frequency/phase detector. The current sources are controlled with a signal, CULCV (Cleanup-loop Compensation), at connector P1 pin 1. This signal controls the phase detector coefficient to compensate for the change in the VCO frequency-voltage coefficient to maintain constant loop bandwidth. The variable resistor R30 allows the matching of the cleanup loop bandwidth to that of the compensation circuit in the main loop phase detector. This matching provides flat angle-modulation frequency response. The optimum bandwidth for the cleanup loop is 30 kHz.

2-245. The output of the frequency/phase detector and switched current source drives the integrating operational amplifier U9. The positive input is biased in the middle of the frequency/phase detector ECL swing. The feedback resistor R37 and capacitor C27 provide a low frequency breakpoint to increase the phase margin of the loop. The output of the operational amplifier U9 passes through the loop filter (C31 through C36 and L6 through L8) and the lead/lag network (R39, R58, R46, and C40) and then to connector J3, pin 1, to the VCO. The loop filter rejects the SSB spurious signals above 200 kHz. Rejection notches are located at approximately 200 kHz, 300 kHz, and 1 MHz. The lead/lag network has a lag break at about 36 Hz and a lead break at about 1450 Hz. This amplifier/filter combination provides good closed loop response and noise performance.

2-246. A speed-up network (double pellet diodes CR8 through CR11, R32, and R45) improves the switching speed for large frequency transitions. This network does not affect normal angle modulation signals because of the conduction voltage of the diodes.

2-247. The cleanup loop VCO frequency stops are formed by operational amplifier U15, diodes CR12 and CR13, and associated resistors. This circuit acts as active diode clamps on the control voltage to the VCO. The resistorR52 is used for adjusting the high end voltage (about 16 volts) corresponding to a high frequency of 535 MHz. The resistor R51 is used to adjust the low end voltage (about 2 volts) for the low end frequency of 235 MHz. These limits prevent loop lock up at frequency extremes where the VCO and divider operation is not predictable.

2-248. A3A7 Sub-Synthesizer PCB Circuit Analysis

2-249. Refer to the System Block Diagram and the A3A7 Syb-Synthesizer PCB Schematic located in the 6070A/6071A Schematic Manual.

2-250. The Sub-Synthesizer generates the lo frequency signal which is summed in the A3A6 Sing Sideband Mixer PCB to produce the five lower orde digits (1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz) of frequenc resolution. This loop is similar to the main loop in that i contains a single sideband mixer and pulse deleter i addition to the usual components of a phase-locked loo (phase detector, VCO and N/1).

2-251. The 10-MHz reference signal from the A3A2 10 MHz Reference PCB is transformed into a narrow puls train by U2. This 10-MHz pulse train provides the inpu to a three-decade rate multiplier consisting of U10, U15 and U20. Integrated circuit U14 is used to compensate fo the propagation delays of the rate multiplier. Th individual rate multiplier provides an output pulse rat (Y) equal to one-tenth the BCD input (A, B, C, D = 1, 2, 4 8). For example, when the BCD input number is 7, ther will be 7 output pulses for every 10 input pulses and th average output frequency is 0.7 times the input frequency lowever, these pulses are not evenly spaced in time. B cascading three rate multipliers, an average frequency of to 9.99 MHz can be generated (U20-6) with a 10-MH input. This is summed with 10 MHz in U21 to produce 1 MHz to 19.99 MHz at U21-1 (TP8). This is divided in tw stages by 100 in U22, and U23, attentuated by L7, C32 R23, R24, and R39, and low-pass filtered by C33, C34 C36, C37, L8, and L9 to produce a 100 to 199.9 kHz sin wave. An active quadrature generator (U30, U31, R21 R22, R33, C23, C25, C40, and C41) generates two signal (TP5, TP6) with a 90-degree phase difference. This is fe into the single sideband mixer via R20, R29, C28, an C29.

2-252. The Sub-Synthesizer VCO consisting of Q6, tan L5-CR1, and associated components has a frequenc range of approximately 80 MHz to 120 MHz. Its output i buffered by an ECL line receiver U34 to feed a divide-by 10, U32, and a divide-by-4, U29. The ECL output of U3 is transformed to TTL by Q1, and Q2 and again divide by 10 in U33 to provide the approximately 0.8 MHz to 1. MHz for the main loop single sideband mixer.

2-253. The divide-by-4, U29 provides two quadratur outputs that drive the LO inputs of mixer U27 and U2 via C26, R40, and C42, R43 respectively. The mixe outputs are summed with R25, R26, and R28 to produce lower sideband (Fc – Fs) signal, where Fs can vary fro 100 kHz to 199.9 kHz. Fc is the carrier signal, 20 MHz t 30 MHz or one-fourth the VCO frequency. This carrie signal is filtered by C46 through C50 and L10, L11 and i coupled into an ECL buffer U25 via C52. This buffer i used as an amplifier, and the ECL output is used to drive an ECL to TTL converter (Q3 through Q5 andassociated components). The TTL output is buffered by U19-6 and i fed into the pulse deleter (U3, U8, and U19-3).

2-254. This pulse deleter removes a pulse from the inpu signal, at U19 pin 6 at every negative transition of U8 pin

13. This causes U8 pin 9 to go high. On the next clock of the input signal, U8 pin 5 goes high, and on the following negative clock U3 pin 7 goes low, preventing the input signal from reaching U19 pin 3 and, therefore, deleting a pulse. As soon as U3 pin 7 goes low, it immediately clears the two previous flip-flops so on the next negative clock U3 pin 7 goes high, and pulses can reach U19 pin 3. This delete signal is supplied by rate multiplier U9 which is driven by the 1-MHz reference to produce delete rates from 0 to 900 kHz in 100-kHz steps.

2-255. The average frequency of the output of the deleter, U19 pin 3 is lower by the delete rate (Fd). This makes the deleter output frequency Fc – Fs – Fd. The deleter output drives the N/1 divider.

2-256. The programmable N/1 divider (U3, U5, U19-11, U19-8, and associated components) divides the deleter output frequency to a single frequency. The CK input of flip-flop U4 goes high when the counter reaches 27. The output of the flip-flop (U4 pin 8) goes low allowing a new number to be loaded into counter U5 on the next clock cycle (count 28). This causes the CK input of flip-flop U4 to go low. On count 29 the count-load line (U5 pin 1) goes high allowing the counter to resume counting. The larger the number that is loaded into the counter, the smaller number of counts the counter will take to reach the terminal count of 29. (i.e., If 0 is loaded the counter will divide by 29, and if 9 is loaded the counter will divide by 20 (a nines complement BCD system.)

2-257. The output of the N/1 is compared with the reference frequency (Fr) in the phase detector (U13 and U18). Since the two frequencies must be the same, the input to the N/1 (Fc – Fs – Fd) must be N*Fr. Therefore, Fc = N*Fr + Fs + Fd. The minimum values for N, Fs, and Fd are 20 kHz, 100 kHz, and 0 kHz, respectively. Therefore (since the reference frequency is 1 MHz) the L0 input to the single sideband mixer has a minimum frequency of 20.1 MHz. The VCO operates at 80.4 MHz and, in this case, the output to the main loop signle sideband mixer is 0.804 MHz. For the maximum values of 20 kHz, 199.9 kHz and 900 kHz, for N, Fs, and Fd respectively, the output is 1.203996 MHz.

2-258. The digital outputs of the phase detector, U18 pin 11, and U18 pin 6, are connected to a differential integrator consisting of U24 and associated components. The integrator output, which supplies the VCO control voltage, is filtered by C13, C14, C17C18, C19 and L3, L4, and is connected to the varactor CR1 to form a closed phase-locked loop. For troubleshooting, SW1 allows the loop to be opened and a fixed tuning voltage to be supplied to the VCO from R5. The operating point of the phase detector is set to approximately 2 radians by a small amount of leak current, from R8, which is summed into U24 pin 2. Under normal operation there should be 200 nS pulses at TP7 and U18 pin 8. These pulses are filtered by R50, C64 to produce approximately 1 VDC. This voltage is compared on the A3A9 Synthesizer Distribution PCB and, if it is outside the window of 0.8V to 1.2V, it indicates a Sub-Synthesizer unlock condition.

2-259. The Sub-Synthesizer is programmed by serial frequency information from the CPU via the A3A9 Synthesizer Distribution PCB and decoded in latches U7, U12, and U17. The information is transferred to the Sub-Synthesizer circuitry via a second level of latches U6, U11, and U16 at a time determined by a signal (TMCNTH) on the A3A4 N/1 Divider PCB.

2-260. A3A8 Synthesizer Control Buffer PCB Circuit Analysis

2-261. Refer to the System Block Diagram and the A3A8 Synthesizer Control Buffer Schematic located in the 6070A/6072A Schematic Manual.

2-262. The A3A8 Synthesizer Control Buffer PCB interfaces the control and status lines to the A3A2 10 MHz Reference PCB, the A3A3 Delay Discriminator PCB, and the A3A4 N/1 Divider PCB. The 10 MHz reference control lines are decoded by the addressable latch U4, and then are buffered by U3. Component U10 is also an addressable latch which is used for decoding the control signals to the A3A3 Delay Discriminator PCB. These control signals are buffered by U11. Data and select signals are buffered through U9 and sent to A3A4 via P2. DAC U6 is set by six bits from latch U1 and four bits from latch U4. The analog output is KNV (Main Loop Gain Compensation Voltage) which goes back through the A3A9 Synthesizer Distribution PCB, and from there goes to the A3A1 Phase Detector. The purpose of this analog voltage is to maintain a constant mainloop bandwidth by compensating for changes in the VCO tuning coefficient and the N/1 division ratio. DAC U7 is set by two bits from latch U1 and all eight bits of latch U2. The analog output is PHV (Phase Shifter DAC Voltage) and goes to the A3A3 Delay Discriminator PCB. Both of these voltages are derived from data stored in the calibration EPROM.

2-263. A3A9 Synthesizer Distribution PCB Circuit Analysis

2-264. Refer to the System Block Diagram and the A3A9 Synthesizer Distribution PCB Schematic located in the 6070A/6071A Schematic Manual.

2-265. All of the digital control lines, BABO to BAB5,, BDTA, BSEL2, BSEL3, BSEL5, and BSEL6, originate from the A2A1 Controller PCB. Some of these control lines are decoded by U2, are buffered through U13, and then are returned to the A3A7 Sub-Synthesizer PCB. Component U10 is an 8-bit addressable latch of which six outputs control the A3A1 Phase Detector through buffer U9. The output from latch U10-4 is used for the most significant bit of DAC U7. Components U1 and U4 are

also addressable latches, of which U4 provides the rest of the bits to U7, and U1 provides an 8-bit word to control DAC U3. DAC U3 provides the compensation voltage CULCV to the cleanup loop on the A3A6 Single Sideband Mixer which passes through the A3A8 Synthesizer Control Buffer and the A3A4 N/1 Divider. The input KVFM signal (Compensated FM Modulation Signal) is applied to DAC U7-15 via J16. DAC U7 provides the analog voltage PDFM which goes to the A3A1 Phase Detector to angle modulate the main loop. Three status lines are conditioned on the A3A9 Synthesizer Distribution PCB: SSPDV, DDINV, and DELVLV. Components U12-1 and U12-2 form a window comparator for SSPDV to produce a digital output SSULK (Sub-Synthesizer Unlocked Status). Component U12-13 digitizes the analog signal DILVLV to DIUNL (Discriminator Unlocked Status). The remaining statusline DDINV (Discriminator Invalid Status) triggers a retriggerable one-shot (U6) which is used as a pulse stretcher to provide a constant low level output DDNR (Discriminator Not Ready). The status indicators N1TST (N/1 cable continuity test bit), RNULK (10-MHz Reference Unlocked Status), and DIUNL (Discriminator Unlocked Status) from the A3A8 Synthesizer Control Buffer; SSULK (Sub Synth Unlocked Status) and STST from the A3A7 Sub-Synthesizer; and RPD (Reduce Peak Deviation Status) from the A3A1 Phase Detector are multiplexed by U11 for reading by the A2A1 Controller PCB.

2-266. A4A2 Modulation Oscillator PCB Circuit Analysis

2-267. Refer to the System Block Diagram and the A4A2 Modulation Oscillator PCB Schematic in the 6070A/6071A Schematic Manual for following the circuit analysis.

2-268. The internal modulation source of the Modulation Osillator is a programmable, low distortion two-integrator or phase-shift oscillator covering 20 Hz to 200 kHz, with overrange to 1 Hz and 255 kHz.

2-269. The time constants of the integrators (U13, U18, and associated components) which determine the output frequency, consist of C13 through C16, and C23 through C26 in conjunction with resistors in hybrids U10 and U14, respectively. Resistors R24, R27, and R28 provide bias current compensation for U13. Capacitors C18 and C28 are for high-frequency compensation of U13 and U18, respectively. The capacitors which determine the frequency ranges for U13 are switched by relay contacts K1B, K2B, and K3B. The capacitors which determine the frequency ranges for U18 are switched by relay contacts K1C, K2C, and K3C. The frequency ranges are listed in Table 2-8.

2-270. Relays K1, K2, and K3 are switched by open collector inverters, U2-2, U2-4, and U2-6, respectively. Diodes CR1 through CR3 protect the inverters from inductive transients. The resistors, which control the fine frequency steps in hybrids U10 and U14, are switched by quad DMOS switches. Resistors R1 and R2 bias the comparators at 1.5V so they can be switched by TTL levels. The bit weight, resistor value, and applicable control line are listed in Table 2-9.

Table 2-8. Frequency Ranges

FREQUENCY RANGE	CAPACITOR	RELAY	RESOLUTION
20 Hz - 199 Hz	C13, C23	K1	1 Hz
200 Hz - 1.99 kHz	C14, C24	K2	10 Hz
2.00 kHz - 19.9 kHz	C15, C25	K3	100 Hz
20.0 kHz - 199 kHz	C16, C26	——	1 kHz

Table 2-9. Resistor Value

BIT WEIGHT	RESISTOR VALUE	CONTROL LINE
128	1.5625 K Ohms	B7
64	3.125 K Ohms	B6
32	6.25 K Ohms	B5
16	12.5 K Ohms	B4
8	25 K Ohms	B3
4	50 K Ohms	B2
2	100 K Ohms	B1
1	200 K Ohms	B0
Note: The resistor value includes the FET on resistance		

2-271. Latches U1 and U2 convert the serial data from the microprocessor bus to parallel TTL.

2-272. A necessary condition for oscillation exists when the gain around the loop in unity and the phase shift is 0 degrees. Since each integrator provides –90 degrees phase shift, amplifier U8 must provide 180-degrees phase shift. Additional circuitry provides a mechanism to control the amplitude by slightly varying the phase shift about 180 degrees. The main feedback signal from U18 is summed into the inverting input with R20. Resistor R21 provides feedback around U8. Capacitor C22 is for high-frequency compensation. Resistors R19 and R23 are an offset voltage adjust circuit. A small amount of quadrature component from U13 is summed into the inverting input of U8 via R12 and into the non-inverting input with a voltage divider consisting of R13, R14, and R16. Resistor R16 is in parallel with the resistance of n-channel FET Q2. Resistors R15, R17 linearize the resistance of the FET Q2 as a function of gate-to-source voltage. By changing

the FET Q2 resistance, the magnitude and sign of the quadrature component summed in canbe varied, causing the amplitude of the oscillation to increase or decrease. The operating point of FET, Q2, which reflects the amount of quadrature component summed in, would be constant as a function of frequency if the integrating circuits of U13 and U18 and the inverters U13 and U18 were ideal. At low frequencies no net quadrature component is summed in, while at high frequencies the operating point changes to match the phase shift change in the loop caused by the nonideal behavior of the operational amplifiers.

2-273. The amplitude level control (ALC) loop consists of U6 and associated components. Operational amplifier U6A with diodes CR4 through CR7 and a portion of resistor pack U19 (10K Ohms) form a four-phase rectifier. The outputs of U18, U13, and U8, provide 0 degrees, 90 degrees, and 180 degrees, respectively. The output of U13 is inverted by U6D to give a 270-degree phase shift. The reference voltage from a 6.4V zener CR8, biased by R8, is summed into U6A by R7 and amplitude adjust potentiometer R6. P-channel FET Q1, controlled from open collector inverter U20 with pull-up U5, provides a means to turn the oscillator off by removing the reference. The voltage from temperature compensation diode CR9, biased by R10, is also summed into U6A with resistor R9. In the steady state, the DC output of U6A is zero.

2-274. If the system is perturbed so that the oscillator amplitude increases, the voltage at the output of U6A will decrease. The voltage at the output of integrator U6B will begin to ramp up, and consequently the voltage to the control FET Q1 will ramp down and tend to turn off the oscillator to maintain a constant amplitude. The reverse happens for an amplitude decrease.The integrator time constant is determined by R11 and C1 through C4. These capacitors are switched by relay contacts K1A through K3A to match the frequency band. Diodes CR10, CR11, and resistor R18 form a speed-up network used to improve the oscillator switching speed. The ALC loop stability is maintained by summing the nonintegrated signal into the noninverting input of U6C.

2-275. Output amplifier U17 has a gain of two and acts as a buffer to feed the front panel output. Resistors R25 and R26 set the gain of U17 and capacitor C22 provides frequency compensation.

2-276. A4A3 Attentuator PCB Circuit Analysis

2-277. Refer to the System Block Diagram and the A4A3 Attentuator Schematic located in the 6070A/6071A Schematic Manual.

2-278. The A4A3 Attentuator PCB provides the basic 6 dB level increments for controlling the instrument output. The total attenuation range, including one section on the A4A7 or A4A6 Output Amplifier PCB, is 0 to 138 dB. This is accomplished with one 6-dB section, one 12-dB section, and five 24-dB sections.

2-279. Control signals determining which attentuator sections are in or out of the circuit come from the A4A10 Modulation Distribution PCB. These TTL control signals are level shifted and applied to Q3 through Q8 which switch the current through the coils of relays K1 through K6. Relays K1 through K6 are DPDT relays wired in a transfer switch configuration. In the off or no coil current condition, the relay contacts are arranged so that the input RF signal enters the relay, goes through the attenuator pad, and exits the relay. In the "on" or coil current applied condition, the input RF signal passes directly through the relay contacts with no attenuation. The attenuator sections are "pi" pads with resistor values selected such that each pad exhibits a characteristic impedance of 50 ohms and the required attenuation factor. The attenuator sections are switched in and out individually in any combination corresponding to the attenuation required by the front panel or remote RF level setting.

2-280. A4A4 Modulator Divider PCB Circuit Analysis

2-281. Refer to the System Block Diagram and the A4A4 Modulator Divider PCB Schematic located in the 6070A/6071A Schematic Manual. The A4A4 Modulator Divider PCB (Mod Divider) is located on the A4 Output Module Plate.

2-282. The 250-MHz to 520-MHz signal from the A3A3 Delay Discriminator PCB enters the Mod Divider at J13 at a level of approximately 8 dBm into the resistive pad (R85, R86, and R87) and then into the junction of the pin diode switches (CR6, CR7, CR8, and CR9). Depending on which frequency band the desired output signal is the appropriate diode will be DC biased into conduction while the other diodes will be biased off. Diode CR8 enables the signal to reach modulator U10 when the frequency lies between 520 MHz and 360 MHz (A-Band). Diode CR7 enables modulator U4 when the signal lies between 360 MHz and 250 MHz (B-Band). If the frequency is between 250 MHz and 62.5 MHz (C, D, E, and F Bands), then diode CR6 enables the signal to reach dividers U15 and U14. For frequencies below 62.5 MHz (G-Band), diode CR9 enables the signal to reach modulator U18 and the A4A9 Heterodyne Converter PCB. The DC bias current to control the diodes passes down the signal lines and is returned to ground through L3 and R12.

2-283. In the fundamental bands (A and B) and the heterodyne band (G), the signal passes directly to the modulators. The hybrid modulators U4, U5, U10, U12, and U18 and dual gate FETs Q2 and Q3 act as wide range variable gain amplifiers to control the amplitude of the signal in response to commands from the automatic level

control (ALC) circuitry and to control amplitude modulation (AM). The output of each modulator passes through a low-pass filter to remove harmonic distortion present on the input signal or the divided signals. The A4A4 Modulator Divider PCB is a three-layer Teflon glass circuit board with each low-pass filter printed as a stripline structure in the center conductor layer. The PCB is covered on both sides by ground plane. The filter for the upper half octave of the fundamental band (A) is located ahead of the output connector J3 and passes all signals from 0.2 MHz to 520 MHz. The lower frequency filters (D, E, and F bands) use external ceramic capacitors as part of the filter structure. The outputs of each band are summed to a common point by pin diode switches CR10 through CR15. The DC bias to enable the output diodes is controlled by the appropriate modulator.

2-284. For a programmed frequency from 125 MHz to 250 MHz, the input signal 250 MHz to 500 MHz is divided by two in digital divider U15. The output of U15 is amplified by hybrid amplifier U13. The output of U13 is switched by pin diodes CR19 and CR20 to the appropriate modulator U5 or U12 and to their respective low-pass filters. When the programmed frequency is within therange of 62.5 MHz to 125 MHz, the 125-MHz to 250-MHz output of U15 is further divided by U14. The output of U14 is amplified by U11 and switched by pin diodes CR23 or CR24 to the gate of the appropriate FET modulator Q2 or Q3 and their respective filters. From switches CR10 to CR15 the signal goes through a high-pass filter and to pin diode switches CR18, CR25, and CR17. For frequencies from 0.2 MHz to 62.5 MHz, the signal is applied to J2 from the A4A9 Heterodyne Converter, then passes through low-pass filter FL1 and CR17 to amplifier U1 and to the output connector J3. The DC bias to enable CR18 and CR25 is controlled by Q5 and associated circuitry Q4 and U3.

2-285. When the output signal is in the heterodyne band, the A4A9 Heterodyne Converter senses the presence of the DC bias and control signal generated by U18 and passes it with the RF signal through connector J1. The A4A9 Heterodyne Converter then generates a DC control signal which comes into J2 and enables diode CR17 to conduct the 0.2-to 62.5-MHz signal to u1 and to the output connector J3.

2-286. The selection of the appropriate band to process the signal is accomplished by decoding the control data from A4A10 Modulation Distribution PCB on lines BAND1H, BAND2H, and BAND4H. The binary coded command is decoded into 1 of 7 by U16 generating 0 to 12 volt control commands on lines "A" through "H". These control commands pass through the appropriate modulator and turn on one of the output diodes CR10 through CR15, or CR2 and U1 on the A4A9 Heterodyne Converter PCB.

2-287. Command lines C through F are used to control dividers U15 and U14, transistor Q1, and input switch diode CR6 by means of diodes CR1 through CR5, CR21, and CR22.

2-288. The BAND control data is also decoded by analog switch U2 which connects the AM/ALC analog control line from the A4A7 Output Amplifier PCB (A4A6 Times Two Output PCB in 6071A only) to the input of the appropriate operational amplifier U6 through U9. These amplifiers generate analog control a through g varying from 0 to +10 volts and control the gain of the appropriate modulator and the bias current through input diodes (CR6 through CR9, CR19, CR20, CR23, or CR24). Control data BAND2H and BAND4H are further decoded by U3 to enable switch diodes CR18 and CR25 when the frequency is between 62.5 MHz and 520 MHz. Potentiometer R88 and selected resistors R3 through R9 are used to set the ALC loop gain in each band, dependent on the modulator transfer function and the total RF gain in each frequency band. Transistor Q6 responds to the "Times 2 Select" command X2SLH from the A4A10 Modulation Distribution PCB when the 6071A is in the 520-MHz to 1040-MHz band. When Q6 is turned off by X2SLH being true, it turns analog switch Q7 off which adds resistor R2 into the analog path to compensate the ALC loop gain in the 520-MHz to 1040-MHz band.

2-289. A4A5 Reverse Power Protection PCB Circuit Analysis (Option -870)

2-290. Refer to the System Block Diagram and the A4A5 Reverse Power Protection PCB Schematic in the 6070A/6071A Schematic Manual. The A4A5 Reverse Power Protection (RPP) PCB provides protection for the 6070A/6071A in the event that excessive RF or DC power is applied to the instrument RF output connector. This protection is valid up to an applied power level of 50watts maximum from a 50 ohm source. Protection from DC voltages up to ±50V DC is also incorporated, subject to the 50-watt maximum power rating.

2-291. There are three basic protection methods incorporated in the RPP. The first method is a diode limiter (CR1 through CR4 and CR11 through CR14). This limiter clamps the voltages applied, including fast rise time or pulsed signals, to a level which will not damage the instrument. The second method is the DC blocking provided by capacitors C17 and C18. The third method is provided by relay K1. When the RF level becomes high enough (approximately 0.5 watts), CR15 detects sufficient voltage to change the state of comparator U1. This causes latch U2 to change state. The change in state will turn off Q2 which turns off Q1 and removes the current drive to the coil of K1. When K1 releases, the RF line to the output connector is shorted to ground, and the RF line back to the instrument is opened. This effectively disconnects the instrument from the RF

output connector. A status signal from the latch, (RPTRPL) is sensed by the microprocessor which flashes the RF OUTPUT ON indicator and performs the RF off function. Pressing the RF OUTPUT ON indicator button will reset the latch U2 through the RPRSTL line if the source of RF power has been removed. Note that if the instrument is in stanby, or unplugged from power, K1 is de-energized and thus is in the disconnect state. The instrument is also protected in the RF OFF condition.

2-292. A4A6 Times Two Output Amplifier PCB Circuit Analysis (6071A Only)

2-293. Refer to the System Block Diagram and the A4A6 Times Two Amplifier PCB Schematic in the 6070A/6071A Schematic Manual. The A4A6 Times Two Output Amplifier PCB amplifies the 0.2-MHz to 520-MHz RF signal, and generates the 520-MHz to 1040-MHz signal. The times two output amplifier circuitry amplifies the signals to the level necessary to obtain the desired instrument output level. The PCB contains much of the automatic level control circuitry (ALC), and contains one attenuator (24 dB) section.

2-294. THE RF SIGNAL PATH

2-295. The 0.2-MHz to 520-MHz input signal comes from the A4A4 Modulator Divider PCB output (A4A4J3) and is connected to the output amplifier at E1E2. Components U1 and U2 are wideband RF amplifiers with approximately 7.5 dB gain each. The output of U2 goes to K1. Relays K1 and K2 are DPDT relays used to route the RF signal directly through to the detector U20 for frequencies less than 520 MHz and through the times two (X2) circuitry to the detector for frequencies of 520 MHz to 1040 MHz. Components T1, Q1, and Q2 and associated circuitry form an active frequency doubler. Transformer T1 splits the RF input signal into two opposite phase outputs which are applied to Q1 and Q2, respectively. The collectors os Q1 and Q2 are tied together summing the outputs. This forms a full-wave rectifier (or doubler). Amplifiers U5 and Q3 are used to control the current through the doubler circuit. As the rf drive level to the doubler increases, the collector current increases. This changes the doubler's gain characteristics. Controlling the current through the doubler tends to hold the doubler's gain constant as the RF drive level is varied. The doubler output goes to U3, a 520-MHz to 1040-MHz amplifier with approximately 7 dB gain. From U3, the RFsignal goes to a switch/bandpass filter matrix. As the signal generated in the doubler contains the input frequency and many unwanted harmonics, it is necessary to filter the signal. Four bandpass filters are required to cover the 520-MHz to 1040-MHz band. Bandpass filter (BPF) 1 is for frequencies between 520 MHz to 600 MHz, BPF 2 is for frequencies between 600 MHz to 720 MHz, BPF 3 is for frequencies between 720 MHz to 875 MHz, and BPF 4 is for frequencies between 875 to 1040 MHz. The drive for the pin diode switches is supplied from U11 through U14. The filtered RF signal is then amplified by U7 and U6 (520-1040-MHz, 7-dB gain amplifiers) and goes to relay K2 where it rejoins the main RF signal path. The signal from K2 goes to the detector U29 and R26. The network R26, C31, and R37 taps off a small (-20 dB) portion of the signal from K2 and connects it to E3E4 where it is available as the auxiliary RF output signal (Option 831). The main portion of the signal goes through the detector U20. The detector introduces approximately 3.5 dB loss to the RF signal. From the detector, the RF signal goes to relay K3, a DPDT relay. In the normal operating mode, the RF signal passes directly through K3. Anytime a signal level is requested which exceeds +13 dBm (or +7 dBm in the X2 band), K3 is energized and the signal passes through U9 which is a wideband RF amplifier with approximately 6 dB gain. This post detector gain block is necessary to reach signal levels greater than +13 dBm (or +7 dBm in the X2 band). From K3, the RF signal goes to K4 which, together with R43, R44, and R45, forms a switchable 24-dB attenuator section. From K4, the RF signal exits the A4A6 Times Two Amplifier PCB at connector J2 and goes to the A4A3 Attenuator PCB.

2-296. AUTOMATIC LEVEL CONTROL (ALC) LOOP

2-297. The detector U20 contains two RF diode detector circuits. One section is used when the RF frequency is less than 5 MHz and the other is used for frequencies greater than, or equal to 5 MHz. The detector circuits are the same except for coupling and bypass capacitor values. Both detectors are on the RF line permanently and their outputs are switched by Q4 and Q5. The detector also contains a temperature compensation diode, the output of which is summed with the detector diode output at the common source of Q4 and Q5. U15 is a buffer amplifier. Amplifier U16, together with the resistor/diode network connected between U16 pin 6 and U16 pin 2, forms a linearization circuit. This circuit takes the output of the detector diode, which is nonlinear with varying power levels, and transforms it to an output which is linear as RF output level is varied. (This is necessary to keep the ALC loop gain relatively constant.) The output of the linearizer goes to U17. Integrated circuit U17 and associated circuitry form the loop integrator. The loop control signal (1+AM), which comes from the A4A10 Modulation Distribution PCB, is summed with the linear detector output at U17, and the error signal (AM/ALC) is applied to the A4A4 Modulator Divider PCB. The error signal is further processed on the A4A4 Modulator Divider PCB and applied to the RF modulators to control the gain of the modulators. The RF output of the A4A4 Modulator Divider PCB is applied to the A4A6 Times Two Output Amplifier PCB and thereby completes the ALC loop. As the detector bandwidth is much lower when frequencies less than 5 MHz are requested, the integrator must set a lower loop bandwidth to obtain stability. This is done by switching capacitors C22, C78, C23, C75 via Q10 and

Q11. These capacitors then parallel the normal integration capacitors C74 and C79, reducing the loop bandwidth by approximately a factor of 10. Integrated circuit U18 and associated circuitryform an unleveled indicator circuit. When the loop error voltage is within the normal operating boundaries, the output of U18 is low. If the loop unlocks, the error voltage goes toward -12V dc, tripping U18. The output of U18 goes to approximately +5V dc. This is sensed by the instrument controller and provides an "Output Amplifier Unleveled Status" (UNLVL) indication.

2-298. COMMANDS/CONTROLS

2-299. The mode of operation controls for the A4A6 Times Two Output Amplifier PCB are provided from the A4A10 Modulation Distribution PCB. The attenuator select line A242 commands the 24-dB attenuator section. A TTL low on this line inserts the attenuator in the circuit; a TTL high removes the attenuator from the circuit. The output amplifier 6-dB gain select line (G6DBH) controls the 6-dB gain block. A TTL high on this line inserts the 6-dB gain block. A TTL low removes the 6-dB gain block. The low heterodyne select line (LOHETH) line controls the detector and loop bandwidth functions. A TTL low on this line corresponds to frequencies 5 MHz and greater; a TTL high on this line corresponds to frequencies less than 5 MHz. The CW select filter (CWFLT) line controls the insertion of a filter capacitor on the 1+AM line. A TTL high on this line adds the capacitor to provide extra noise filtering when in the CW mode; a TTL low removes the capacitor allowing AM control signals to reach the loop. Doubler Select X2SL inserts and removes the doubler circuit from the RF path. This is programmed high when frequencies of 520 MHz or greater are selected. Doubler filter select FLSL1 and FLSL2 control the selection of the bandpass filters in the times two mode. The two command lines are decoded in U10 to select one of the four filters. The level control reference voltage 1+AM is the composite level control, and AM control analog voltage.

2-300. A4A7 Output Amplifier PCB Circuit Analysis (6070A Only)

2-301. Refer to the System Block Diagram and the A4A7 Output Amplifier PCB Schematic in the 6070A/6071A Schematic Manual. The A4A7 Output Amplifier PCB amplifies the RF signal to the level necessary to obtain the desired instrument RF output level. The amplifier contains much of the automatic level control (ALC) circuitry, and contains one attenuator (24 dB) section.

2-302. RF SIGNAL PATH

2-303. The RF Input signal (0.2 MHz to 520 MHz) comes from the A4A4 Mod Divider PCB (A4A4J3) and is connected to the output amplifier at E3E4. Components U1 and U2 are wideband RF amplifiers with approximately 7.5 dB gain each. The signal from U2 goes to the detector (U3) and resistor R1. The network R1, C43, and R3 taps off a small (-20 dB) portion of the signal from U2 and connects it to E1E2 where it is available as the auxiliary RF output signal (Option 831). The main portion of the signal goes through the detector U3. The detector function is discussed under the heading ALC Loop. The detector introduces approximately 3.5-dB loss to the RF signal. From the detector, the RF signal goes to K1, a DPDT relay. In the normal operating mode, the RF signal passes directly though K1. Any time a signal level is requested which exceeds +13 dBm, relay K1 is energized and the signal passes through U6. Amplifier U6, together with the attenuator pad (R50, R51, R52), forms a 6 dB gain block. This post detector gain block is necessary to reach signal levels greater than +13 dBm. From relay K1, and RF signal goes to relay K2 which (together with resistors R31, R32, and R33) forms a switchable 24-dB attenuator section. From relay K2, the RF signal exits the output amplifier PCB (J2) and goes to the A4A3 Attenuator PCB.

2-304. AUTOMATIC LEVEL CONTROL (ALC) LOOP

2-305. The detector U3 contains two RF diode detector circuits. One section is used when the RF output frequency is less than 5 MHz and the other is used for frequencies greater than, or equal to, 5 MHz. The detector circuits are the same except for coupling and bypass capacitor values. Both detectors are on the RF line permanently, and their outputs are switched by Q1 and Q2. The detector also contains a temperature compensation diode, the output of which is summed with the detector diode output at the common sourceof Q1 and Q2. Amplifier U5, together with the resistor/diode network connected between U5 pin 6 and U5 pin 2, forms a linearization circuit. This circuit takes the output of the detector diode, which is nonlinear with varying power levels, and transforms it to an output which is linear as RF output level is varied. (This is necessary to keep the ALC loop gain relatively constant.) The linear output goes to U7. U7 and associated circuitry form the loop integrator. The loop control signal (1 + AM), which comes from the A4A10 Mod Distribution PCB, is summed with the linearized detector output at U7 and the error signal (AM/ALC) is applied to the A4A4 Modulator Divider PCB and to the RF modulators that control the gain of the modulators. The RF output of the A4A4 Modulator Divider PCB is applied to the A4A7 Output Amplifier PCB input (A4A7E3E4), thereby completing the ALC loop. The detector bandwidth is much lower for frequencies less than 5 MHz, thus, when these frequencies are requested, the integrator sets a lower loop bandwidth to obtain stability. This is done by switching in capacitors C35, C52, C24, and C51 via Q4 and Q5. These capacitors then parallel the normal integration capacitors C23 and C25 reducing the loop bandwidth by approximately a factor of 10.

2-306. Integrated circuit U9 and associated circuitry form an unleveled indicator circuit. When the loop error voltage is within the normal operating boundaries, the output of U9 is low. If the loop unlocks (loses control), the error voltage goes toward -12V dc, tripping U9. The output of U9 goes to approximately +5V dc. This is sensed by the instrument controller and provides an Output Amplifier Unleveled Status (UNLVL) indication.

2-307. COMMANDS/CONTROLS

2-308. The mode of operation controls for the A4A7 Output Amplifier PCB are provided from the A4A10 Modulation Distribution PCB. The attenuator select line A242 commands the 24-dB attenuator section. A TTL low on this line inserts the attenuator in the circuit; a TTL high removes the attenuator from the circuit. The output amplifier 6-dB gain select line (G6DBH) controls the 6-dB gain block. A TTL high on this line inserts the 6-dB gain block. A TTL low removes the 6-dB gain block. The low heterodyne select line (LOHETH) controls the detector and loop bandwidth functions. A TTL low on this line corresponds to frequencies 5 MHz and greater; a TTL high on this line corresponds to frequencies less than 5 MHz. The CW select filter (CWFLT) line controls the insertion of a filter capacitor on the I+AM line. A TTL high on this line adds the capacitor to provide extra noise filteringwhen in the CW mode: a TTL low removes the capacitor, allowing AM control signals to reach the loop. I+AM is the composite level control and AM control voltage.

2-309. A4A8 Heterodyne Oscillator PCB Circuit Analysis

2-310. Refer to the System Block Diagram and the A4A8 Heterodyne Oscillator PCB Schematic that is located in the 6070A/6071A Schematic Manual. The A4A8 Heterodyne Oscillator PCB serves two purposes. It provides direct coupled frequency modulation (DCFM) capability at all output frequencies and serves to heterodyne the synthesizer signal from the fundamental band to the lowest frequency, or heterodyne band. The board is located on the inside plane of the Output Module.

2-311. When the instrument is first turned on, broadband noise is amplified by the amplifiers in the oscillator loop (Q3, U13, U20, U21 and associated components). This noise is filtered preferentially at 520 MHz by the Surface Acoustic Wave Delay Line (SAWDL), U12, and continues to build in amplitude until the limiting level is reached (in the same manner as any conventional oscillator). Part of the signal is split off at the output of the low noise amplifier (Q3) by the 3 dB hybrid coupler (W1). This signal is adjusted to the desired level by a resistive pad, and buffered by U14 before being output at J1 to the A4A9 Heterodyne Converter PCB. The rest of the signal is amplified by U20, which is followed by a resistor pad to adjust signal level and to insure a proper termination for the amplifier. The next hybrid coupler (W2) splits the signal into two output ports. The signal from one W2 port is amplified by U21, passes through a mechanically switched phase shifter (used in initial setup and for long term aging compensation), is amplified by U13, and is fed to the SAWDL, thus completing the oscillator loop.

2-312. The signal from the other W2 port is amplified by U18, and fed to the divide-by-52 circuit. The divide-by-52 output of 10 MHz is presented to phase detector U19 along with a 10 MHz reference derived from the instrument's master clock (A3A2 PCB). The phase detector output goes to the loop filter, half of U23, and through an FET switch (U11) to be summed with the temperature compensation signal at the input to the other half of U23. The output of this amplifier is applied to the electronic phase shifter, closing the phase locked loop (PLL). The electronic phase shifter, used for both phase locking and DCFM, is connected to the remaining port of the hybrid coupler W2. Modulation signals are applied to the input port of the coupler through an isolating RF choke. Board temperature is sensed by a thermistor, and the compensation signal is conditioned by U6. This circuitry also provides a frequency centering function used during alignment.

2-313. The Control Logic (Q1, U7, U8, U15) and the Center Frequency Calibrate (CF Cal) circuitry set up board operation depending upon the presence of the command signals for DCFM (DCFML) or heterodyne band (HETL). When DCFM operation is required, the line identified as DCFM is brought low. This results in the generation of two output pulses by the dual monostable multivibrator (U7). One of these pulses (about 4 microseconds in duration) is used to initialize the CF Cal circuitry. The other pulse (about 140 milliseconds long) is first used to enable a clock generator (U1). The output pulses from clock generator U1 are counted by a binary counter composed of U2and U9. As this counter counts up, its output is converted to a ramp signal by the digital to analog converter U3 and U4. The ramp voltage is compared by U10 to the voltage present at the output of the PLL filter loop (U23-1). When these voltages are equal, the comparator (U10-7) output changes state and stops the clock, thus freezing the counter, and thereby the ramp. A short time later, the 140-ms pulse comes to an end, allowing the FET switch, U11 to change position, substituting the frozen ramp voltage for the previously existing PLL control voltage. Thus, when going to the DCFM mode, the oscillator is no longer phase locked to the 10-MHz standard, but its frequency is held to very nearly the same value. This is done because if frequency modulation was attempted while locked, the modulation frequency response would be adversely affected by the PLL action. At the same time, the unneeded incoming 10-MHz standard signal is turned off by Q1, which sends a command back to the source via the signal line, thus

preventing possible spurious signal generation. At this time the instrument software also enables the modulation signal path, and the A4A8 Heterodyne Oscillator frequency will be modulated accordingly. For all instrument output frequencies not in the Het band, the output from this board is the variable 10 MHz output at J5. This signal is then used as the reference for the main synthesizer, thus modulating the output frequency of the instrument. This line is disabled at the receiving end when not required, to minimize spurious outputs. When operating in the heterodyne band, the control line identified as HETL is brought low. Unless DCFM is also commanded, there is no effect on the board. If DCFM is commanded, at the end of the CF Cal cycle, the divide-by-52 circuit is turned off, because now the output is taken from J1 and used in the A4A9 Het Converter to mix with the synthesizer signal to produce the output signal directly.

2-314. As the amplitude versus frequency characteristics of the SAWDL exhibit substantial unwanted responses above and below the desired frequency, precautions must be taken to insure that operation occurs only at the desired point. This is complicated by the fact that the power supply voltages do not come up exactly at the same time during turn-on, which allows control voltages to momentarily exist outside their normal ranges. This can result in the oscillator coming up on an incorrect frequency, outside the control range of the PLL. To eliminate this possiblity, the instrument software causes a CF Cal cycle (by exercising the DCFML line) at turn-on after allowing time for the power supplies to settle down.

2-315. A4A9 Heterodyne Converter PCB Circuit Analysis

2-316. The A4A9 Heterodyne Converter mixes frequencies from the A4A8 Heterodyne Oscillator PCB and the A4A4 Modulator Divider PCB, and the frequency difference is applied back to the A4A4 Modulator Divider PCB. Refer to the System Block Diagram and the A4A9 Heterodyne Converter Schematic located in the 6070A/6071A Schematic Manual.

2-317. The 520-MHz local oscillator signal from the A4A8 Heterodyne Oscillator enters the A4A9 heterodyne Converter PCB at a level of approximately 7 dBm. The signal is applied to gate 1 of dual gate DMOS FET amplifier Q2, then travels through C11 matching capacitor to gate 2 of DMOS FET Q1. The output of Q1 goes into a printed stripline resonator that is tuned by capacitor C15. The resonator output goes through a printed stripline low-pass filter and a resistive matching pad into the local oscillator inputof double balanced, high level mixer U2 at a level of approximately +17 dBM. Potentiometers R42 and R6 adjust the gain of amplifiers Q1 and Q2 by varying bias conditions.

2-318. The bias on gate 1 of Q1 and gate 2 of Q2 is switched to turn off the local oscillator signal to the mixer when the A4A9 Heterodyne Converter is not used.

2-319. The 457-MHz to 520-MHz linear input (RF) signal to the mixer enters through A4A9 pin 1 from the A4A4 Modulator/Divider PCB. A DC control current is drawn by the Modulator/Divider when the Heterodyne Converter is enabled. This control current is sensed by comparator U1 and associated circuitry and switches on the local oscillator amplifier and the output amplifier. This variation of the DC control current varies conduction of diode CR2, which in turn varies the level of the signal into the mixer. Inductors L3, L12, and capacitor C9 form a high-pass filter to supress the feedthrough of the amplitude modulation. A printed stripline low-pass filter supresses harmonic components on the RF input to mixer U2.

2-320. The output of mixer U2 consists of the undesired sum frequency component which is resistively terminated in R23 and R46. The desired difference frequency component of 0.2 MHz to 62.5 MHz goes through low pass filter L4, and L6, amplifiers Q4 and Q5, low-pass filter L7 and L8, and out through A4A9P2 to the A4A4 Modulator/Divider. A DC control current is fed from the A4A4 Modulator/Divider when the A4A9 Heterodyne Converter is enabled.

2-321. A4A10 Modulation Distribution PCB Circuit Analysis

2-322. Refer to the System Block Diagram and the A4A10 Modulation Distribution PCB Schematic located in the Schematic Manual. The A4A10 Modulation Distribution PCB provides processing for the AM (including level) and FM audio modulation signals. Also, all control bits for the other output plate circuit boards are latched and distributed from this board.

2-323. The audio input form the A1A1 Front Panel Assembly or the A6 Rear Panel Assembly is AC coupled with C1, C2 to a termination resistor R15. The DCCUPH bit controls relay K3 which allows DC coupling. Quad DMOS switch U33 routes the audio signal from the external input or internal modulation oscillator (J2 pin 1) to either the FM depth DAC U25 (EXTFMH, INTFMH) or the AM Depth DAC (EXTAMH, INTFMH). This switch is controlled from latch U38, with level shifter U35 converting the TTL levels to ±12V. When the delay discriminator is switching, DDNRL is asserted (low) which inhibits the FM modulation with gate U36.

2-324. The FM depth DAC U25 is a 10 bit CMOS multiplying DAC, or digitally controlled attenuator, which provides fine control of the FM modulation index, or deviation (MDFMO-9H). These multiplying DACs produce a current, I01 (U25 pin 1), equal to the voltage input, VR (U25 pin 15), divided by the DAC ladder

resistance, multiplied by N/2n, where n is number of bits in the DAC and N is the binary input to the DAC ($0 \leq N \leq 2n-1$). This current output is connected to the inverting input of the operational amplifier U26 pin 2. The feedback RF (U25 pin 16) resistor, which is the same resistance as the DAC ladder, is internally connected in the DAC to IO1. This resistor supplies current from the output of the operational amplifier, U26 pin 6 via an attenuator network (R8, R11, and R14) which also determines the scale factors. This attenuator network, which is in the feedback path, increases the gain of the circuit over what it would be if the feedback resistor Rf were directly connected to the output of the operational amplifier. In this case, the gain with FETs Q5 and Q6 off is –4 (4/5 scale factor). With Q6 on (SFX1H set high), the gain is –5 (1 scale factor). With Q5 on (SFX54H set high) and Q6 off, the gain is –6.25 (5/4 scale factor). These scale factor bits are used to compensate for various combinations of FM deviation ranges and RF frequency bands. For example, in the fundamental band, 250 MHz through 519 MHz, the gain is –5. Potentiometer R41 adjusts the offset voltage and C13 is used to compensate the high frequency response. Schottky diode CR10 protects the DAC from power turn-on voltage transients.

2-325. The output of the FM depth circuitry is connected to a selectable ±1 gain stage consisting of U23 and associated circuitry. When Q7 is on, the noninverting input, U23 pin 3, is grounded and U23 is a conventional inverting operational amplifier with R18 the input resistor and R17, R44 the feedback resistors. When the FET is open the input signal appears at the noninverting input, U23 pin 3. The same signal must appear at the inverting input, U23 pin 2. Since no current can flow into the operational amplifier, the output signal must equal the input signal, a gain of +1. The gain is nominally set to –1 by programming the FMINUL bit high, which makes the phase of the signal to the KV DAC (J10) the same as the input, except when in the heterodyne band (RF out <62.5 MHz). The ± gain balance is set by R44. Resistors R46 and R61 provide offset adjustment in the –1, +1, mode, respectively. Capacitors C23 and C31 provide frequency compensation.

2-326. The output of the ±1 gain amplifier U23 is connected to the KV DAC on the A3A9 Synthesizer Distribution PCB and to the noninverting input of the DCFM buffer, U18 pin 2, with R45 and FET Q10. When HETMDL is asserted (low), Q10 is on and Q11, a p-channel FET, is off. This path is used when in the heterodyne band where the modulated A4A8 Heterodyne Oscillator output at 520 MHz is mixed with the unmodulated synthesizer plate output to produce a signal in the 0.2 MHz to 62.5 MHz region.

2-327. The audio from the ±1 gain amplifier is also connected to an equalization network (U19, U24, and associated components). This network, which compensates for the effect of the tracking phase-locked loop following the signal sideband mixer, is identical to that on the A3A1 Phase Detector PCB. The output of this network is connected to a multiplying DAC U12 which compensates for the multiplication factor of the synthesizer phase-locked loop. When the synthesizer is operating at 250 MHz and has a FM deviation of 100 kHz, the DCFM oscillator deviates 4 kHz with respect at 10 MHz, a multiplication factor of 25. When operating at 500 MHz, the DCFM oscillator deviates 2 kHz. The NIDAC is programmed to 960 and 480, respectively, to reflect the required 2:1 change in deviation as a function of frequency. The output of the NI DAC, U19 pin 1, is connected to the DCFM buffer, U18 pin 1, via R35, R48 and FET Q4. When REFMDL is asserted (low), Q4 is on, and Q3 is off. The REFMDL signal path is used when not in the heterodyne band where the modulated A4A8 Heterodyne Oscillator output at 10 MHz provides the reference to the synthesizer via the A3A1 Phase Detector PCB. The REFMDL signal path provides DCFM for modulation rates which are inside the main phase locked loop bandwidth. Resistor R48 adjusts the DCFM deviation. For rates outsidethe loop bandwidth, the modulation occurs on the A3A3 Delay Discriminator PCB. Resistors R43 and R50 adjust the offset voltage for the equalization network and NI DAC respectively.

2-328. The DCFM buffer is an inverting amplifier which provides the FM ranging and adjustment for the A4A8 Heterodyne Oscillator PCB. FET Q8 is closed except in the 500 kHz range where it is opened to increase the gain by a factor of 2. Potentiometer R33 adjusts the 500-kHz deviation, and the R31 adjusts all other frequency range deviations. The other ranges are determined by hybrid U41, relays K1, K2, and DMOS switch U1. The controlled frequency ranges are shown in Table 2-10. (Additional range control, outside the loop bandwidth, for DCFM on the non-heterodyne bands is covered in the A3A3 Delay Discriminator PCB Circuit Analysis, and range control for ACFM cases is covered in the A3A1 Phase Detector PCB Circuit Analysis.)

2-329. The relays are controlled by U10, and the DMOS switch is controlled by U2. The output of the buffer is sent to the A4A8 Heterodyne Oscillator PCB. Potentiometer R54 is for offset voltage adjust.

2-330. The input signal is also coupled to the AM Depth DAC (AMDO-9H), U27 pin 15, U28 and associated circuitry. This DAC, which controls the percent AM modulation, is similar to the FM depth DAC in that there is an attenuator network (R47 and R27 in parallel with R22 and R21) in the feedback path. This stage has a gain of approximately –1.33 at 100 percent AM (AMD = 1000).

2-331. Part of this network is used to sum a DC reference voltage from zener CR8 with the input signal.

Potentiometer R22 adjusts the AC/DC ratio or percent AM modulation. The input signal plus DC reference, which represents (1 + am), is connected to the level DAC input, U29 pin 17. This 12-bit DAC (LEO-11H), in conjunction with operational amplifier U30, controls the vernier RF output level. The four most significant bits are latched separately in U22 and are clocked to the level DAC by the LECHKH bit to minimize level glitches. This stage has adjustable gain from -1 to -2 for level calibration (with R25). This signal provides the reference for the instrument ALC loop on the A4A7 Output Amplifier PCB or A4A6 X2 Output Amplifier PCB.

Table 2-10. Frequency Range Control

RANGE	BIT	CONDITIONS
500 kHz	HETRN5H	Q8 open, K1 closed
250 kHz	HETRN4H	Q8 closed, K1 closed, all others open
100 kHz	HETRN3H	Q8 closed, K2 closed, all other open
50 kHz	HETRN2H	Q8 closed, U1-3 closed, all others open
25 kHz	HETRN1H	Q8 closed, U1-6 closed, all other open
10 kHz	HETRN0H	Q8 closed, U1-11 closed, all others open

2-332. The serial data (BDTAH) and low order address bits (BABOH,1H,2H) from the A2A1 Controller PCB are buffered by U11 and sent to all the latches (74LS259). The three high order address bits (BAB3H,4H,5H) are connected to a pair of 1-out-of-8 decoders, U39 and U40 which are selected by BSEL6L and BSEL5L respectively. The outputs of the 1-out-of-8 decoders are used to enable the various latches. By using this hierarchy, any bit can be set. The outputs of the latches which are connected to other PCBs are buffered by U9, U6, and U17.

2-333. 6070A/6071A Power Supply

2-334. INTRODUCTION

2-335. The 6070A/6071A Power Supply is made up of a basic power supply and associated voltage regulators located in the rear panel assembly. The following description is a circuit analysis of the 6070A/6071A PowerSupply. The power supply contains the following printed circuit boards: A5A1 Power Supply Assembly, A5A2 Power Supply Regulator Assembly, A5A3 Auxiliary Transformer Assembly, A5A4 Input Rectifier Assembly, A5A5 Switching Transistors Assembly, and A5A6 Power Supply Capacitor Assembly. The voltage regulators are A6A2 Series-Pass Motherboard, A6A3 +5 Volt Series Regulator, and the A6A4 +12V, -12V, +24V Series-Pass Regulator. The schematics for the power supply and the voltage regulators are located in the 6070A/6071A Schematic Manual.

2-336. The 6070A/6071A uses a high efficiency switching power supply followed by conventional series-pass regulators to minimize heat dissipation in the instrument. The switching power supply uses pulse-width modulation to control its output as its ac line voltage changes. This makes it possible to maintain a minimum amount of voltage across the pass transistors in the series-pass regulator. The power supply can operate from various line power configurations. Line power voltage can be from 90V to 132V AC rms or from 180V to 264V AC rms. Line frequency can be 47 Hz to 63 Hz. The power supply is usually factory set to operate with a line voltage of 90V to 132V AC rms. The 6070A/6071A has a voltage selection switch located on the rear panel adjacent to the main power fuse. For 180V to 250V AC rms operation, the voltage selection switch must be set to the 230V position.

2-337. SWITCHING POWER SUPPLY OVERVIEW

2-338. Figure 1-3 in the 6070A/6071A Schematic Manual shows the block diagram of the entire power supply. AC voltage is applied to the bridge/doubler rectifier CR1 through a RFI line filter. The rectified output voltage charges the energy storage capacitors, CR3, CR4, and this raw DC voltage is fed, through a common mode noise filter, to the switching power transistors. The switching transistors and the energy storage capacitors form a half-bridge configuration.

2-339. Line voltage regulation is provided by the pulse width modulator. The operation of the pulse width modulator is such that as the AC line voltage goes up, the pulse width becomes narrower, and as the AC line voltage goes down, the pulse width becomes wider. A typical voltage waveform at the primary side of the switching transformer is shown in Figure 2-10.

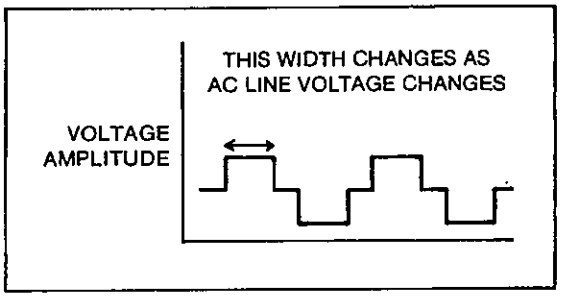

Figure 2-10. Typical Voltage Waveform, Primary Switching Transformer

2-340. The current waveform is similar to the voltage waveform and the amplitude is proportional to the power supply load current. The same voltage waveform appears at the secondary windings of T3 with voltage amplitude equal to the voltage at the primary multiplied by the transformer's turns ratios. The secondary output is full-wave rectified and is fed to the ripple suppression filter where the switching frequency and its harmonic components are filtered. Then each DC voltage is brought to the output terminal through a common mode noise filter.

2-341. The voltage regulation is achieved by monitoring the rectified +6 volt line. The output of the +6 volt rectifier is filtered by a ripple rejection filter (L2 through L6), and fed to an error amplifier U2 where this output voltage is compared against the reference voltage set by R7. This yields a control voltage to the pulse width modulator. The pulse width modulator (U1) provides pulses whose widths are inversely proportional to the control voltage. The output pulses from the pulse width modulator are appliedto switching transistors (Q1, Q2) through transformers (T1, T2). The switching transformer and driver transformer maintain isolation between AC line and chassis ground.

2-342. In order for this power supply to start, an auxiliary power supply, A5A3, provides +12V through CR8 to energize the pulse width modulator error amplifier (U1) before it transfers to the switching power supply output (+13V DC) through CR11 of A5A2. The A5A3 Auxiliary Power Supply also provides +24V DC to the oven oscillator (Option -130) when the instrument power cord is connected to AC line power and the rear panel POWER switch is set to ON.

2-343. Overload protection is provided in this power supply by monitoring the primary current (with T4) of the switching transformer. As soon as the current sense level exceeds the preset reference level (due to a fault or other overload) the pulse width modulator is disabled and the switching action is stopped. This overload condition is sampled at an interval of approximately two seconds, and the power supply is returned to normal operation as soon as the overload condition is removed.

2-344. Due to the limited amount of inductance available for the ripple suppression filter, the power supply output should be loaded with appropriate loads when the power supply is disconnected from the rest of the instrument. The minimum load requirements are listed in Table 2-11.

2-345. Either the synthesizer plate or the output plate is adequate to satisfy the minimum load requirement. If neither of these plates are connected, the dummy loads shown in Figure 2-11 are recommended.

Table 2-11. Minimum Load Requirements

OUTPUT	CURRENT (mA)
+6V/+5V	100 mA
-13V/012V	200 mA
+25V/+24V	98 mA

2-346. SERIES-PASS REGULATORS OVERVIEW

2-347. Refer to the Schematics for the following printed circuit boards: A6A2 Series-Pass Motherboard PCB, A6A3 +5 Volt Series-Pass Regulator PCB, A6A4 +12V, -12V, +24V Series-Pass Regulator PCB and the Power Supply Assembly Schematic. These schematics are located in the 6070A/6071A Schematic Manual.

2-348. Nominally +6V, +13V, and +25V dc are each applied to their respective pass transistors. Zener diode CR1 is used to create a reference voltage for the +24 volt regulator, which in turn provides the reference for the other regulators. The output of the +24V DC line is monitored and compared with the reference voltage at the error amplifier U3 whose output is negatively feedback to the pass transistor Q5.

2-349. The +24V DC is used as the reference voltage to a +12 volt regulator through a voltage divider. The +12 volt regulator is monitored and compared the same way as the +24 volt regulator. The +12V DC line is then used as the reference voltage to the -12 volt regulator and all +5 volt regulators. Operation of these regulators are essentially the same as the +12 volt and +24 volt regulators. The output voltages of all series-pass regulators are monitored for possible shorts in the loads. If the output of a regulator is shorted to ground, the switching power supply output voltages are reduced to a safe level that the pass transistor can withstand. When the short is removed, the power supply resumes its normaloperation.

2-350. The instrument also features a thermal shutdown circuit which is located on the controller (A2A1 PCB in the front panel assembly). When the internal temperature exceeds the preset temperature, the output signal of this circuit disables the pulse width modulator, and the instrument goes into standby until the temperature drops several degrees. Then the instrument resumes its operation.

2-351. A5A4 INPUT RECTIFIER PCB CIRCUIT ANALYSIS

2-352. The schematic for the A5A4 Input Rectifier is located in the 6070A/6071A Schematic Manual.